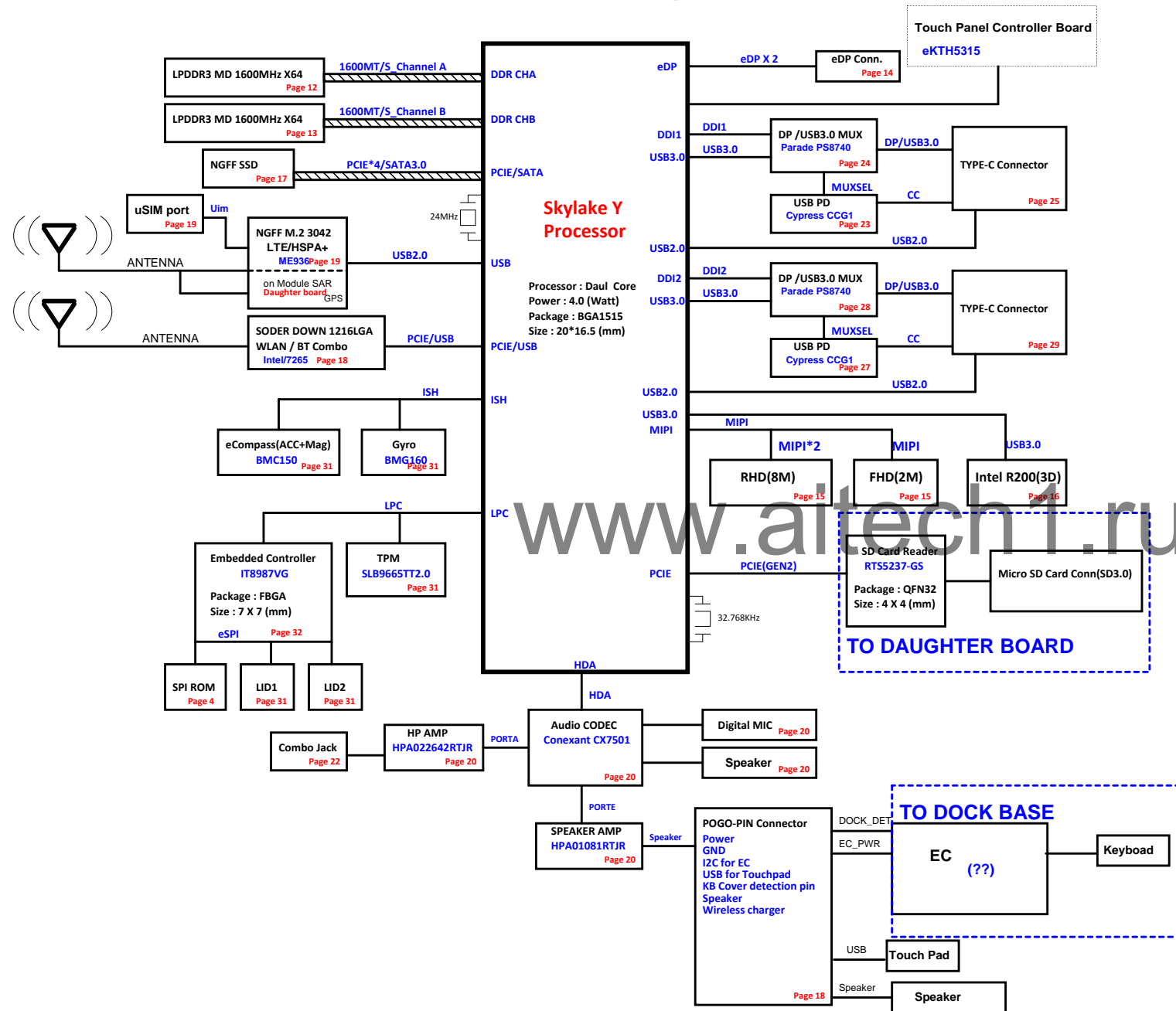
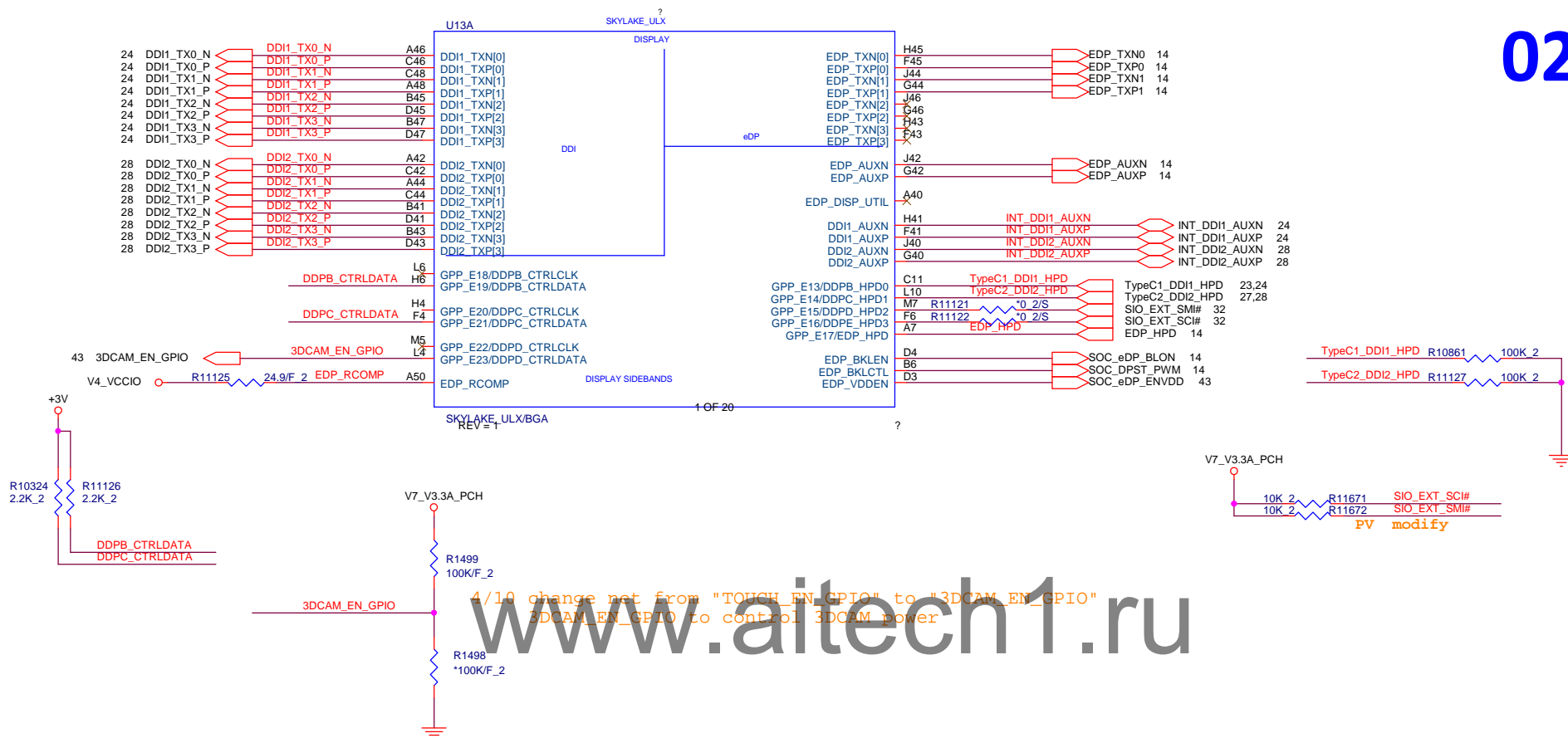


Millhone Block Diagram

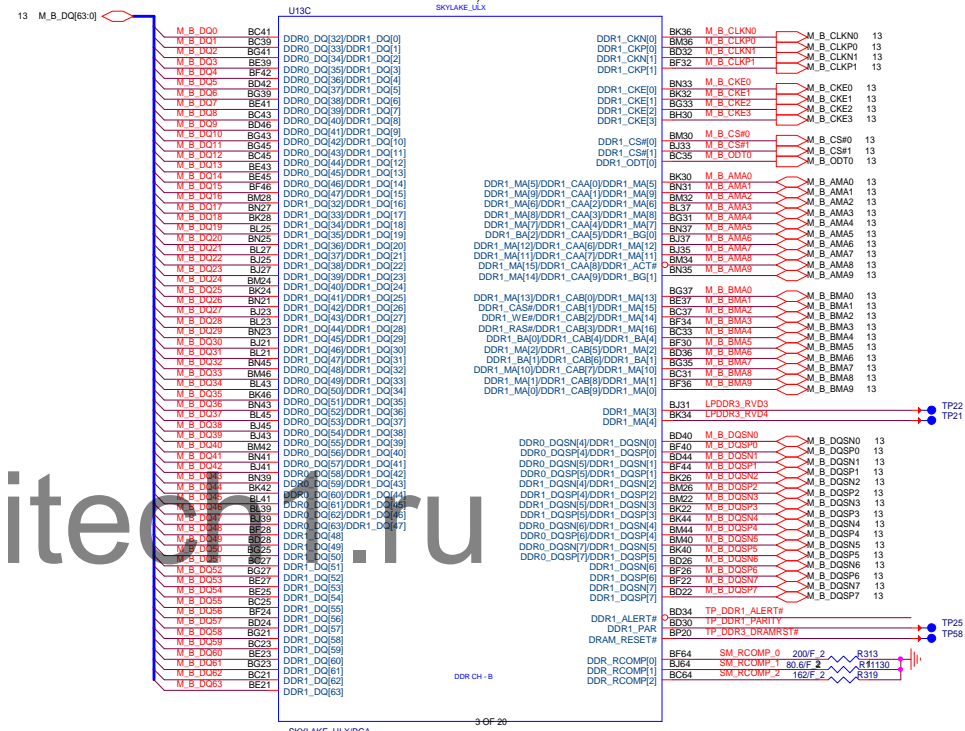
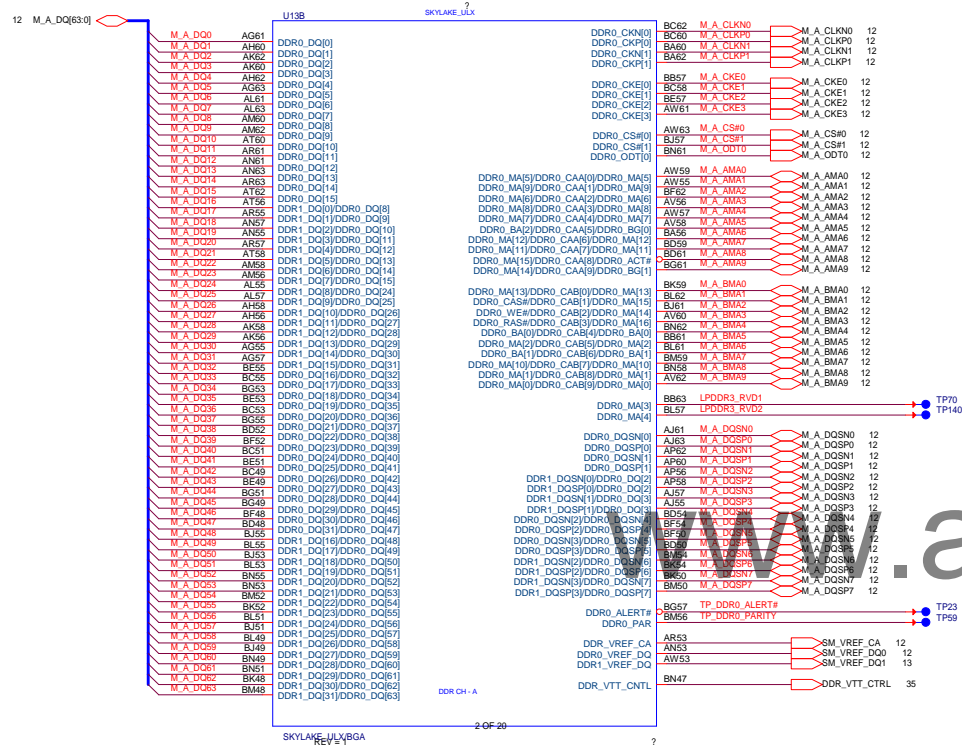
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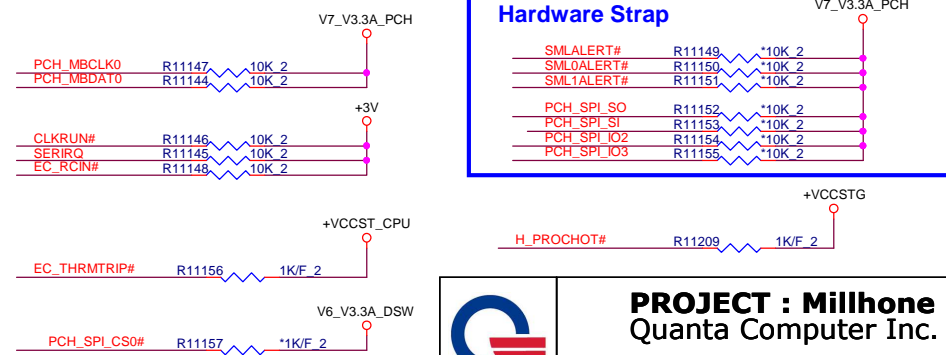
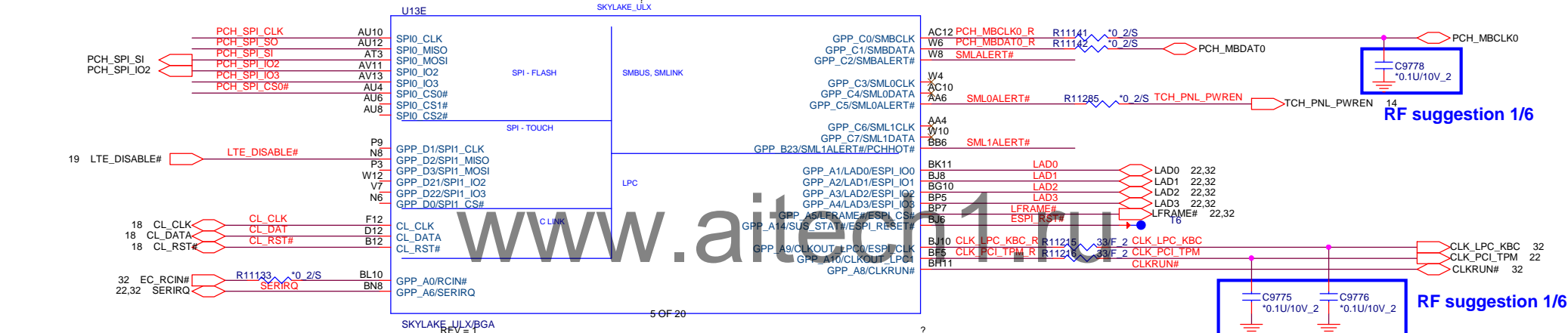





PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (DD/EDP)	A
Date:	Friday, August 28, 2015	Sheet 2 of 48

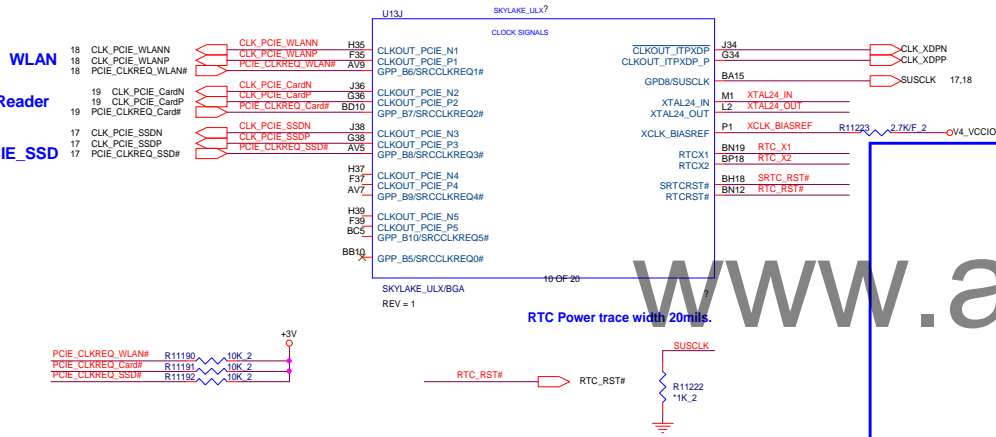
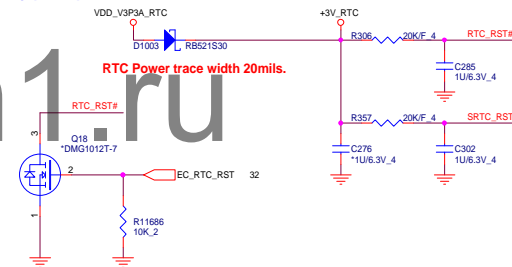
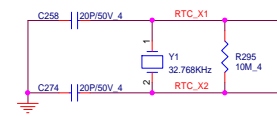
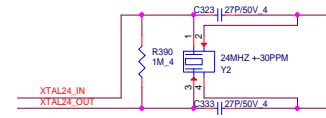
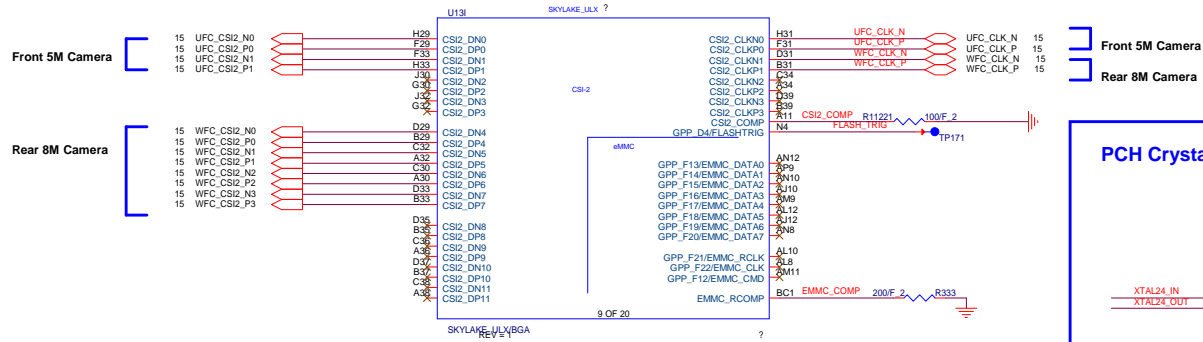


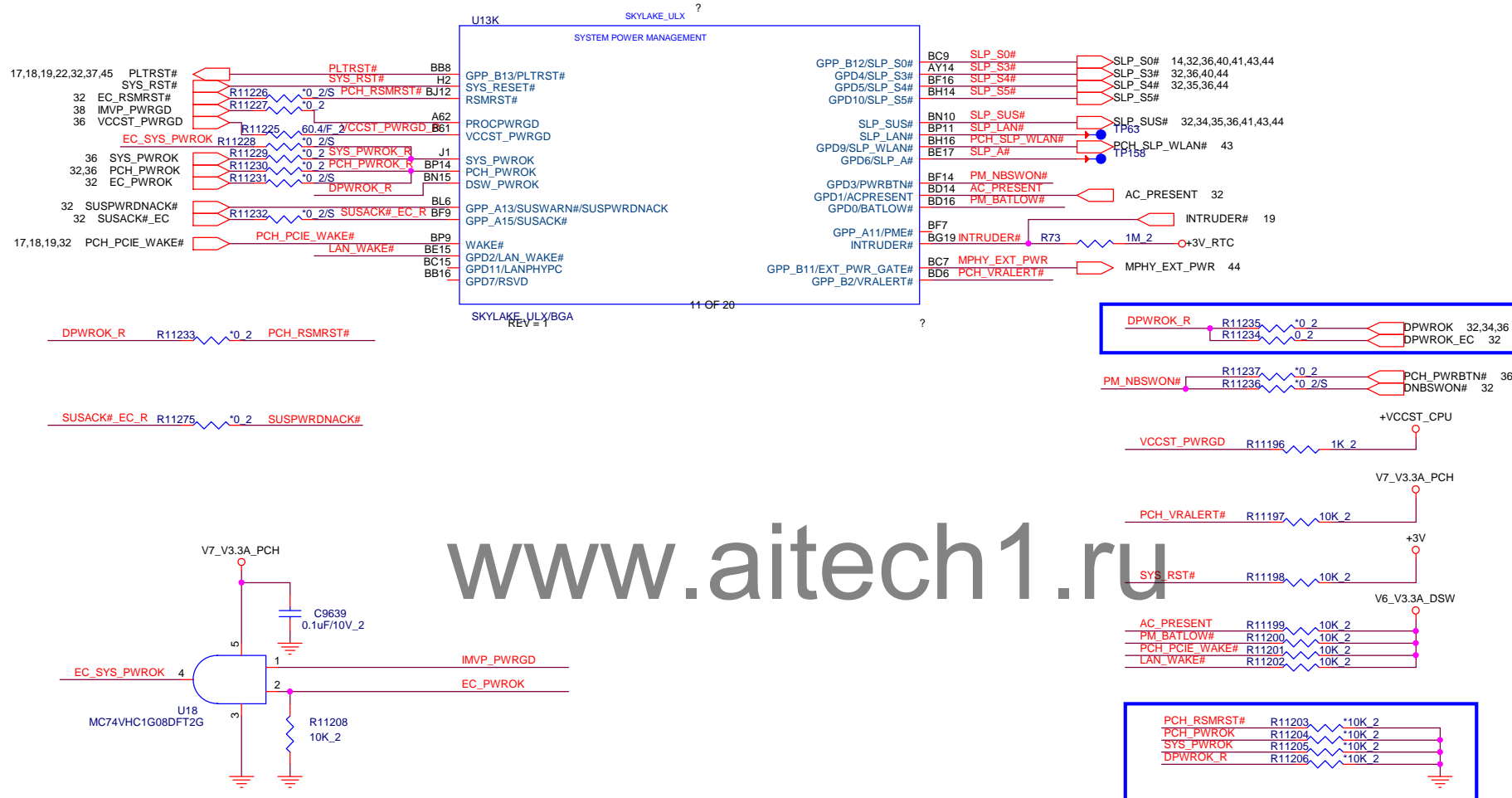


	PROJECT : Millhone Quanta Computer Inc.		
	Size	Document Number	Rev
	SKL-Y CPU (MISC/JTAG/SMB)		A
	Date: Friday, August 28, 2015	Sheet	4 of 48



Size	Document Number SKL-Y CPU (PCIE/USB3)	Rev A
Date: Sunday, August 30, 2015		Sheet 6 of 48





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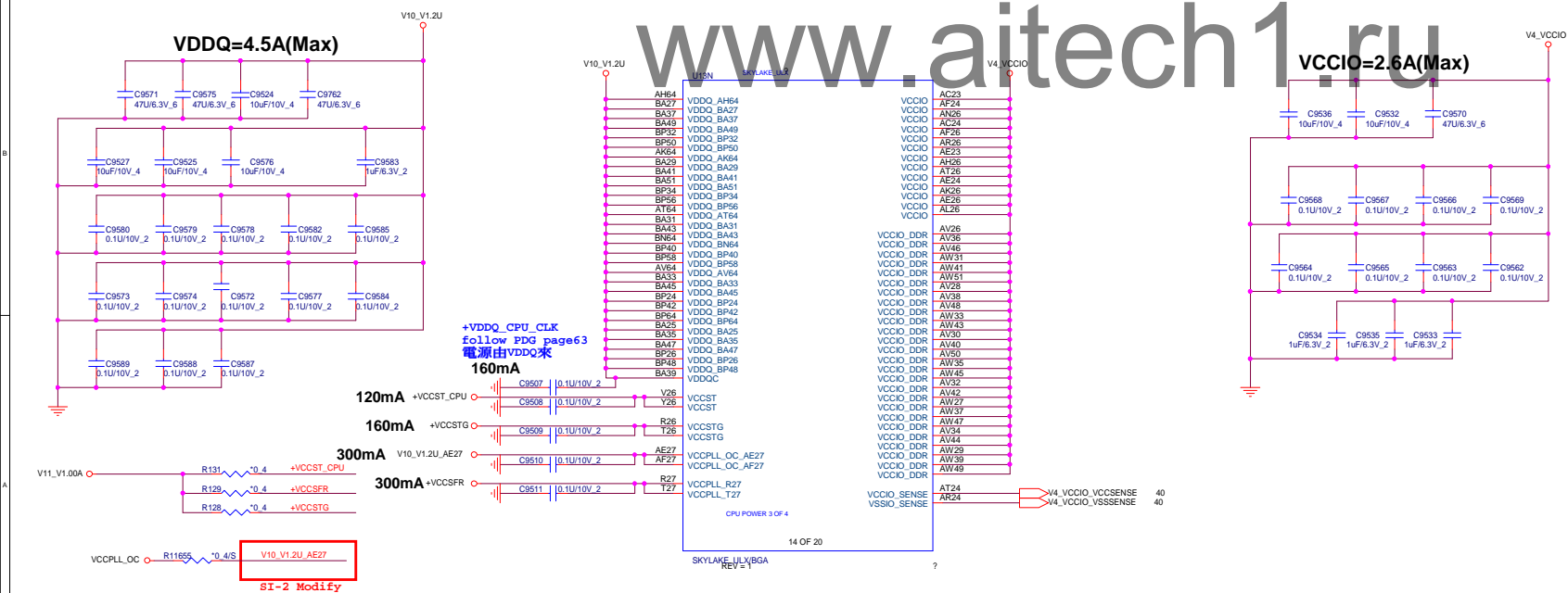
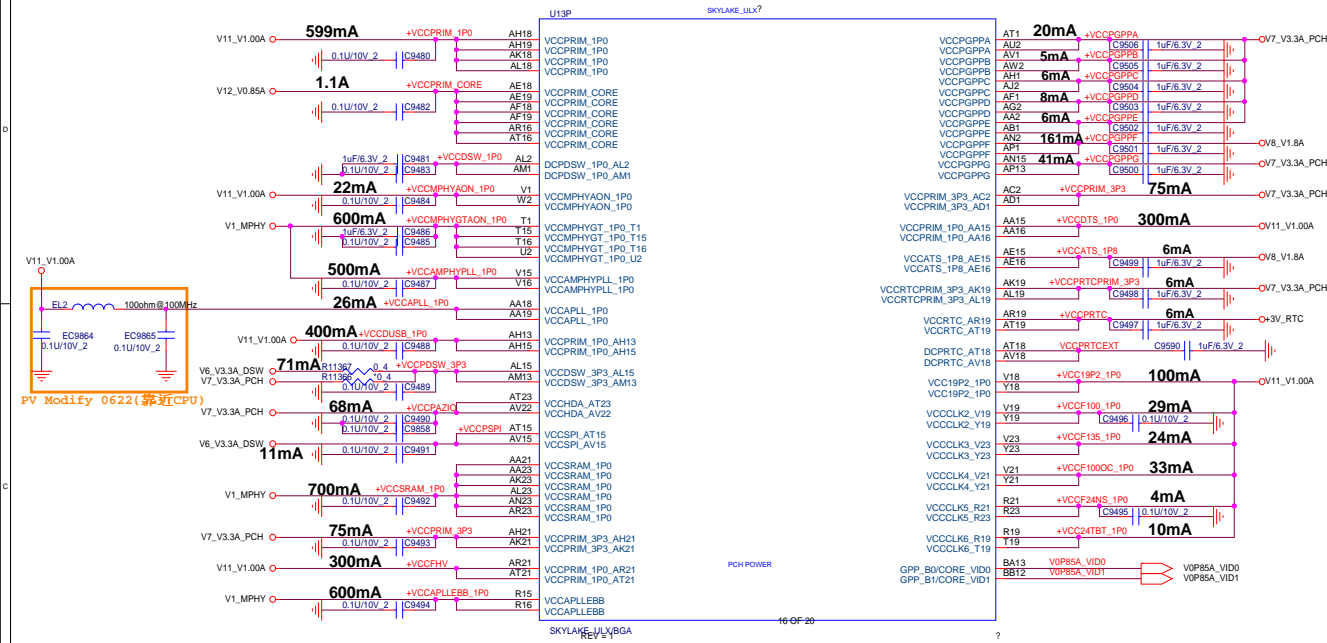


NB5
HW

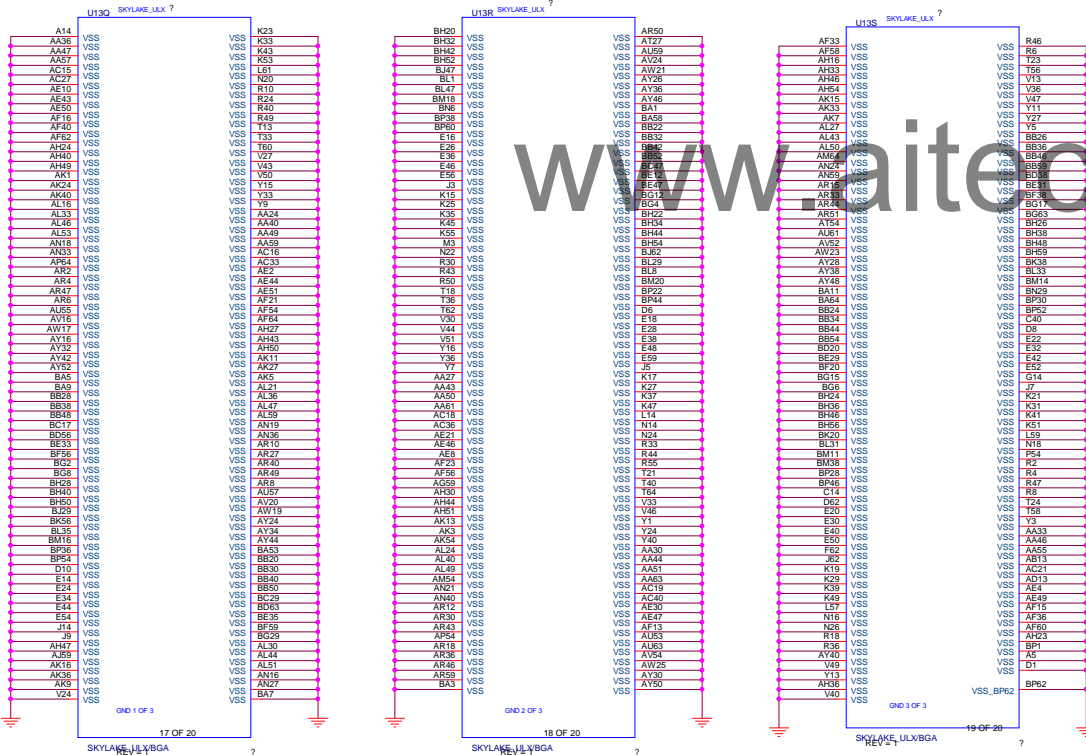
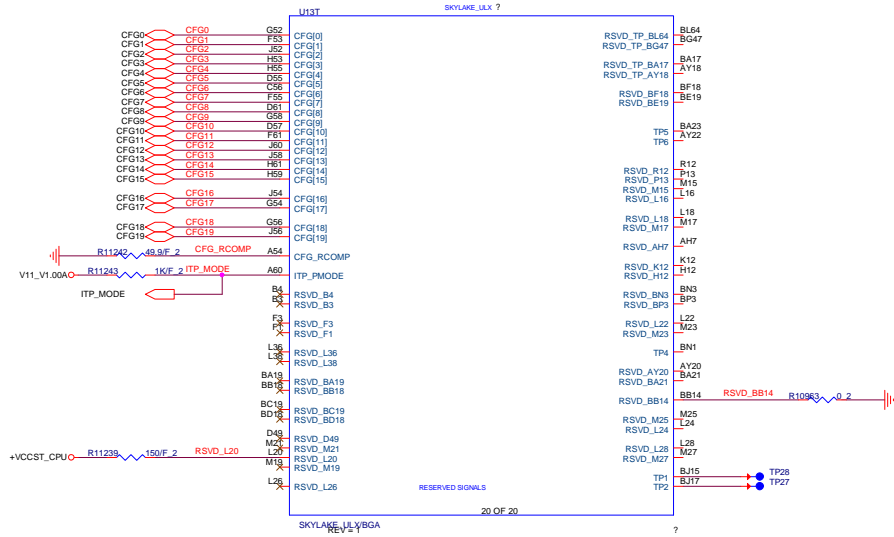
PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (PWR MANAGE)	A
Date:	Friday, August 28, 2015	Sheet 8 of 48





Processor Strapping



	1	0	
CFG4 eDP Enable	DISABLED	ENABLED	
SPKR / GPP_B14	ENABLED	DISABLED	5.20 AC2_SPK
GSP10_MOSI /GPP_B18	ENABLED	DISABLED	5 No_Reboot
SMBALERT# /GPP_C2	ENABLED	DISABLED	Already Pull-high on Page.4
Boot BIOS Strap Bit /GPP_B22	LPC	SPI	(default:SPI)
SML0ALERT#/ GPP_C5	ESPI	LPC	Already Pull-high on Page.4(default:LPC)
SML1ALERT#/ PCHHOT#/ GPP_B23			Already Pull-high on Page.6
SPI0_MOSI			Already Pull-high on Page.4
SPI0_MISO			Already Pull-high on Page.4
SPI0_IO2			Already Pull-high on Page.4
SPI0_IO3			Already Pull-high on Page.4
HDA_SDO/ I2S_TXD0	DISABLED	ENABLED	Already Pull-high on Page.5
Security Flash Descriptors			
DDPB_CTRLDATA /GPP_E19	ENABLED		Already Pull-high on Page.2
DDPC_CTRLDATA /GPP_E21	ENABLED		Already Pull-high on Page.2

Security Flash Descriptors



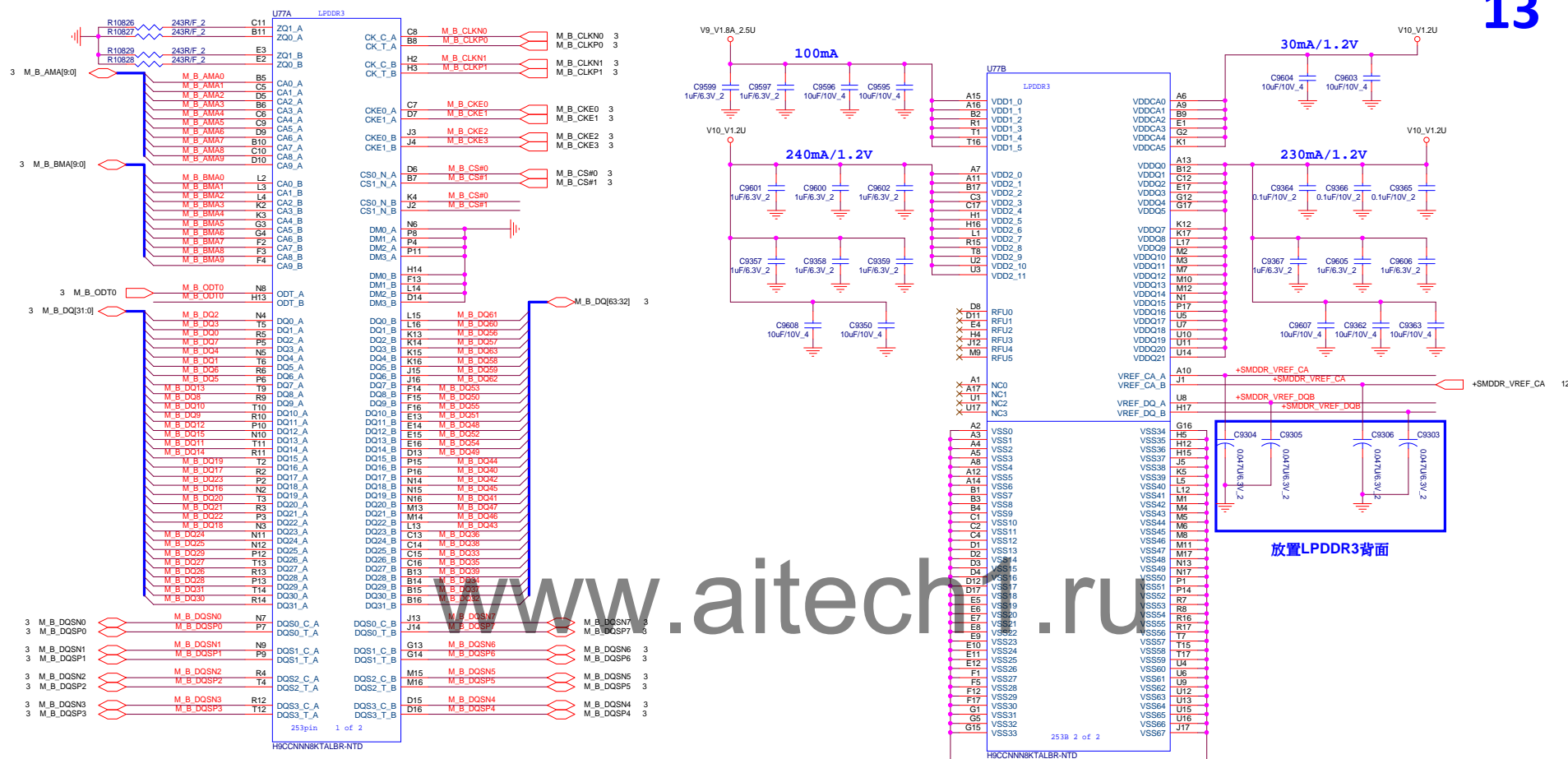
PROJECT : Millhone
Quanta Computer Inc.

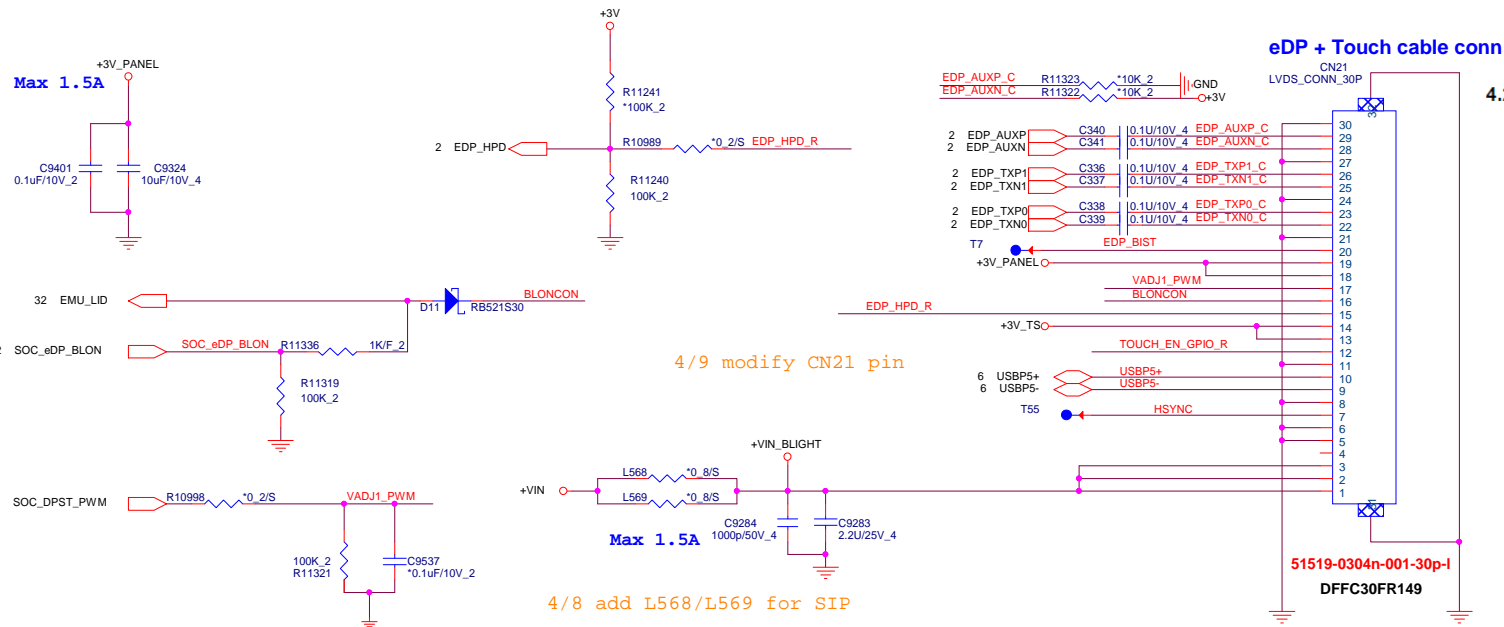
Size	Document Number SKL-Y CPU (VSS/CFG/RSVD)	Rev A
Date:	Friday, August 28, 2015	Sheet 11 of 48



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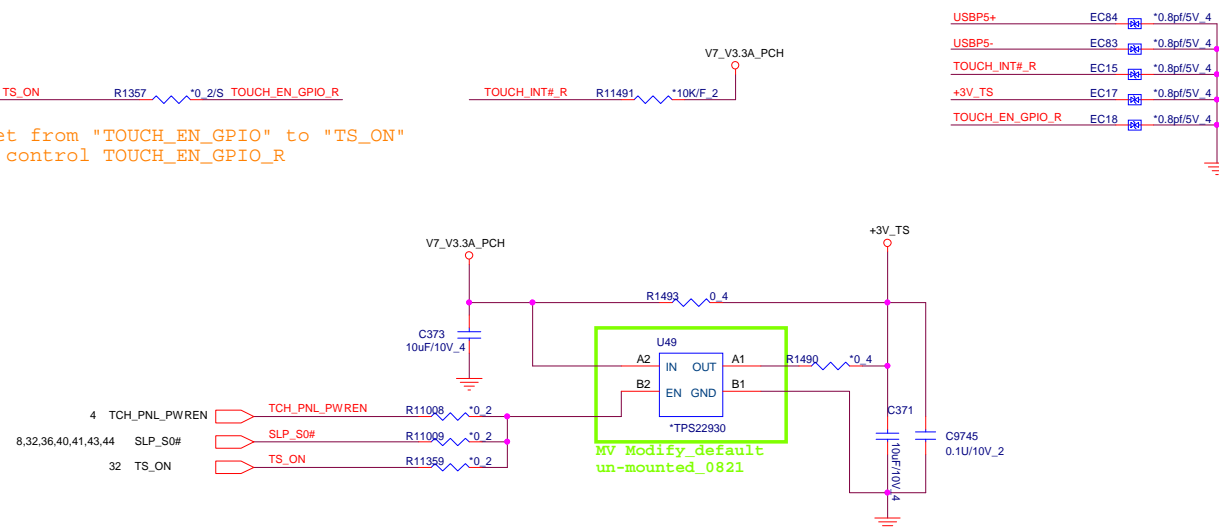
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description
1	NC	No Connection (Reserved)
2	H_GND	High Speed Ground
3	LANE1_N	Complement Signal Link Lane 1
4	LANE1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	LANE0_N	Complement Signal Link Lane 0
7	LANE0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	VCCS	Power Supply +3.3 V (typical)
13	VCCS	Power Supply +3.3 V (typical)
14	BIST	LCD Panel Self Test Enable
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	Backlight Ground
19	BL_GND	Backlight Ground
20	BL_GND	Backlight Ground
21	BL_GND	Backlight Ground
22	LED_EN	Backlight Enable Signal of LED Converter
23	LED_PWM	PWM Dimming Control Signal of LED Converter
24	NC	No Connection (Reserved)
25	NC	No Connection (Reserved)
26	LED_VCCS	Backlight Power
27	LED_VCCS	Backlight Power
28	LED_VCCS	Backlight Power
29	LED_VCCS	Backlight Power
30	NC	No Connection (Reserved)

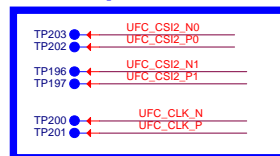
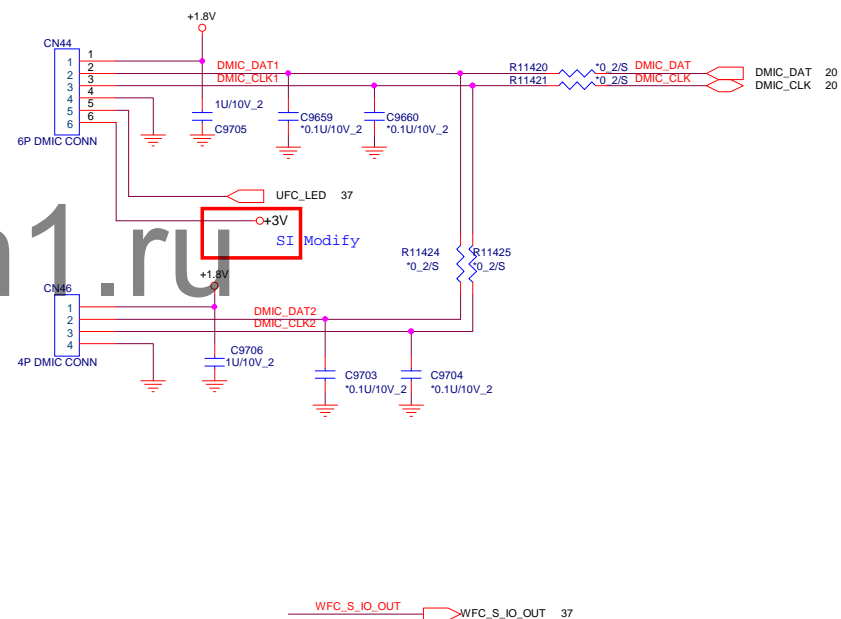
4/10 change net from "TOUCH_EN_GPIO" to "TS_ON"
TS_ON to control TOUCH_EN_GPIO_R

Touch Panel ESD

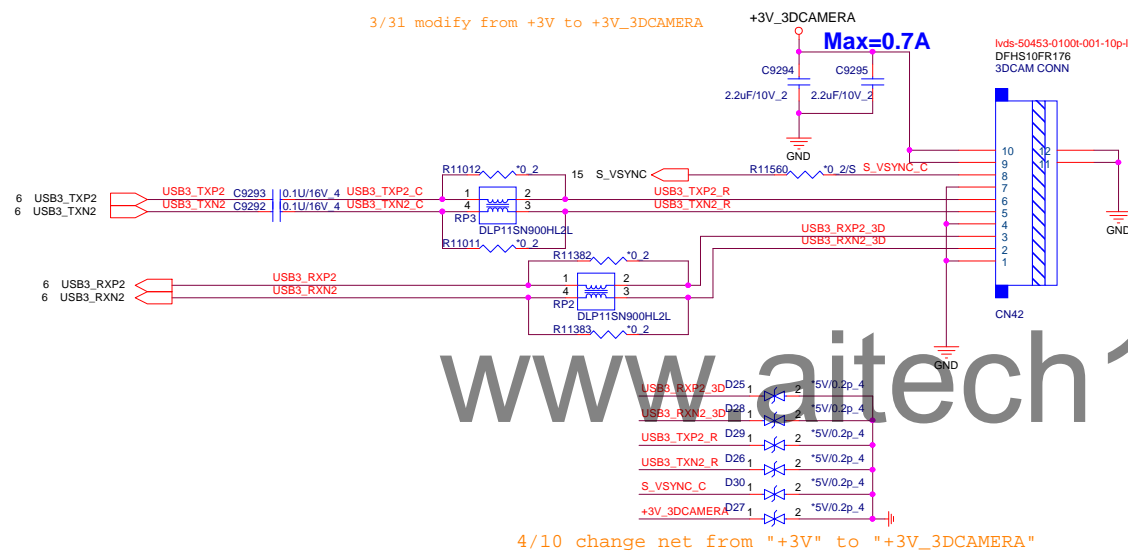


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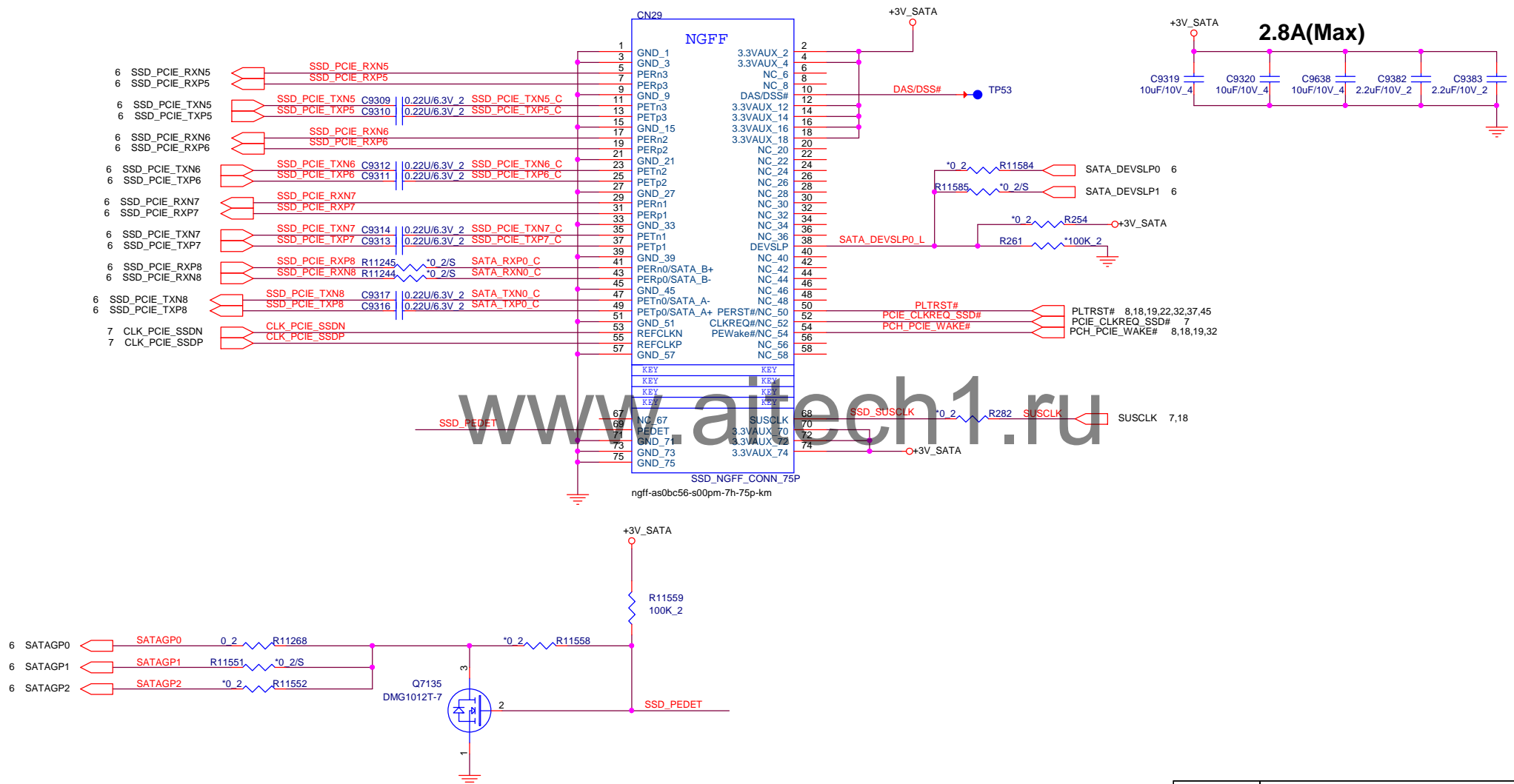
Size	Document Number	Rev
	eDP	A
Date:	Friday, August 28, 2015	Sheet 14 of 48



Intel R200 3D camera

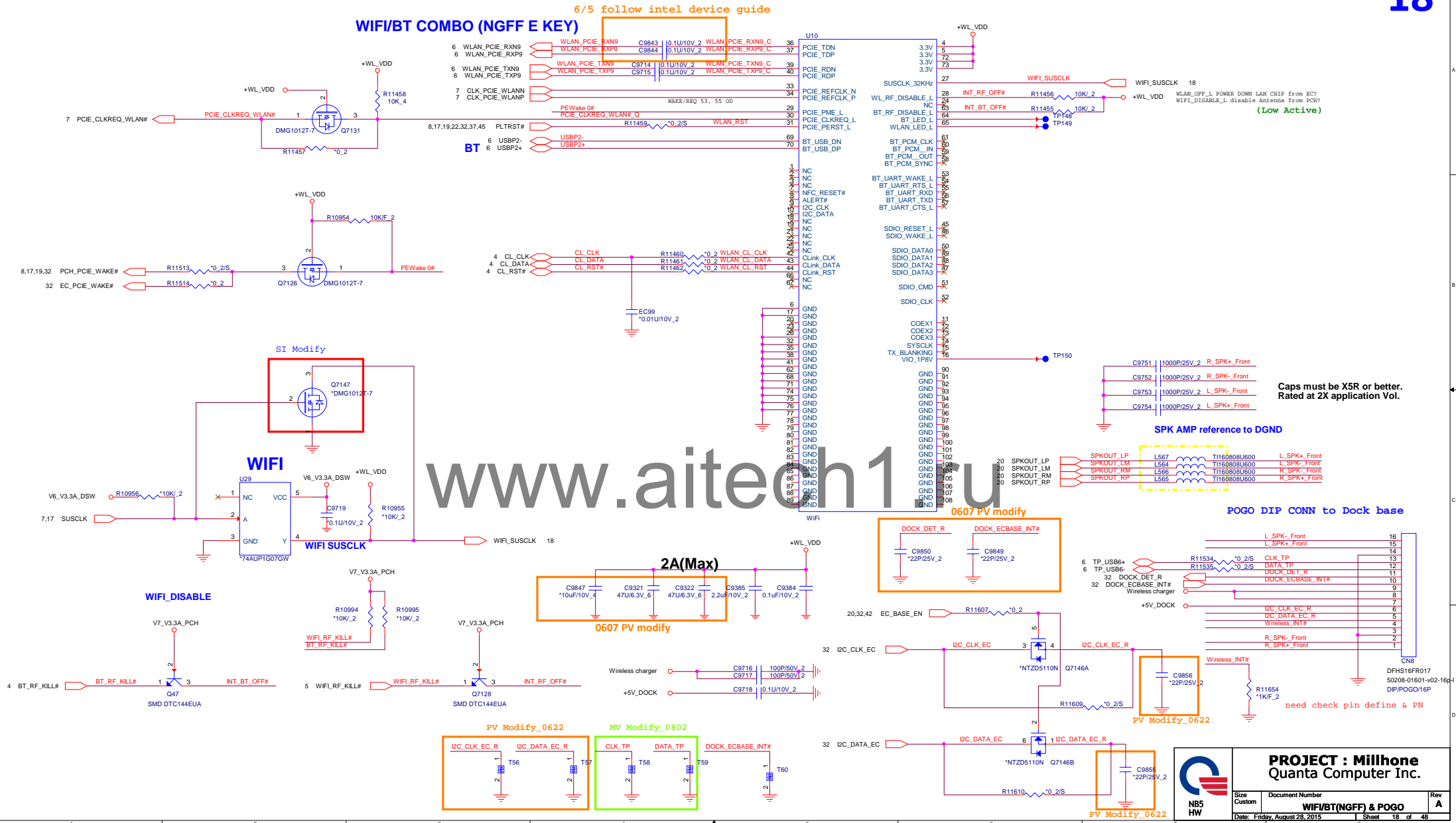


CONN: M KEY MODULE: N/A

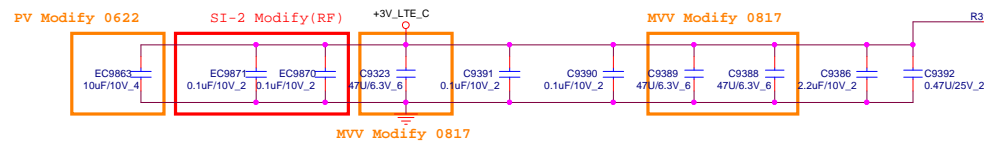
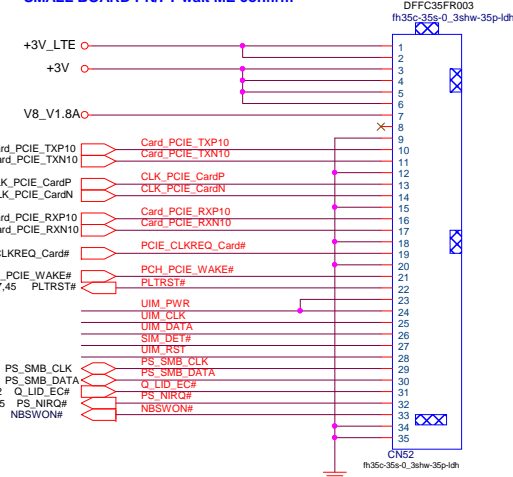
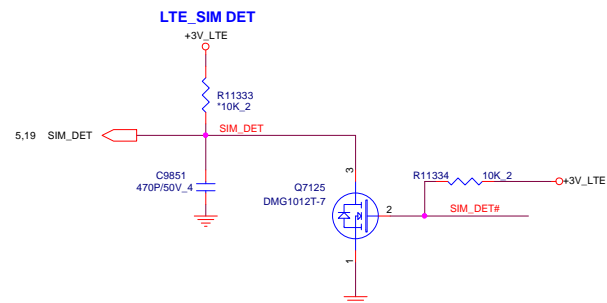


PROJECT : Millhone
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Size	Document Number	Rev
	SSD (NGFF CONN)	A
Date: Friday, August 28, 2015	Sheet 17 of 48	




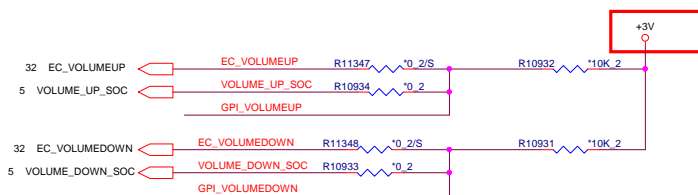
19



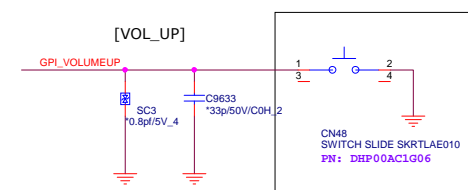
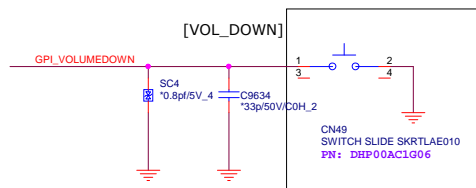
+3V_LTE 19,43
+3V_LTE_C

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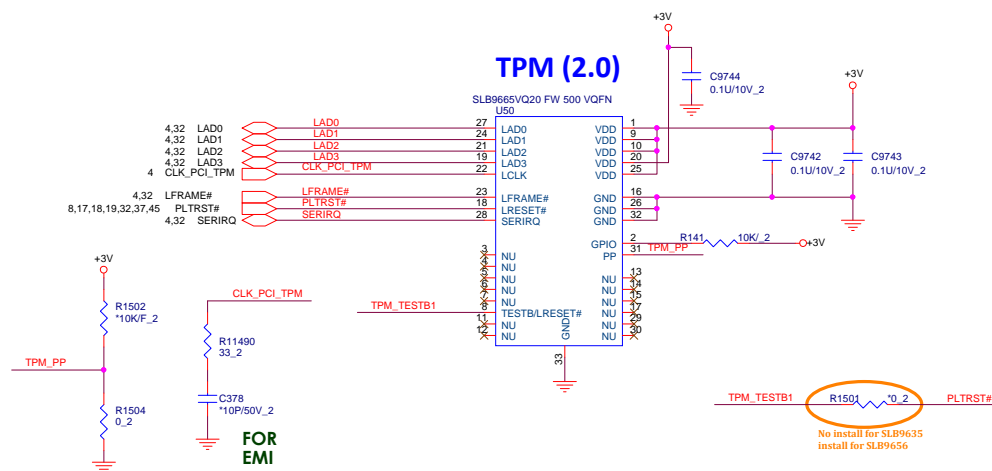
 NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
	Size	Document Number	Rev
		NA	A
Date: Friday, August 28, 2015		Sheet 21 of 48	



Volume BTN



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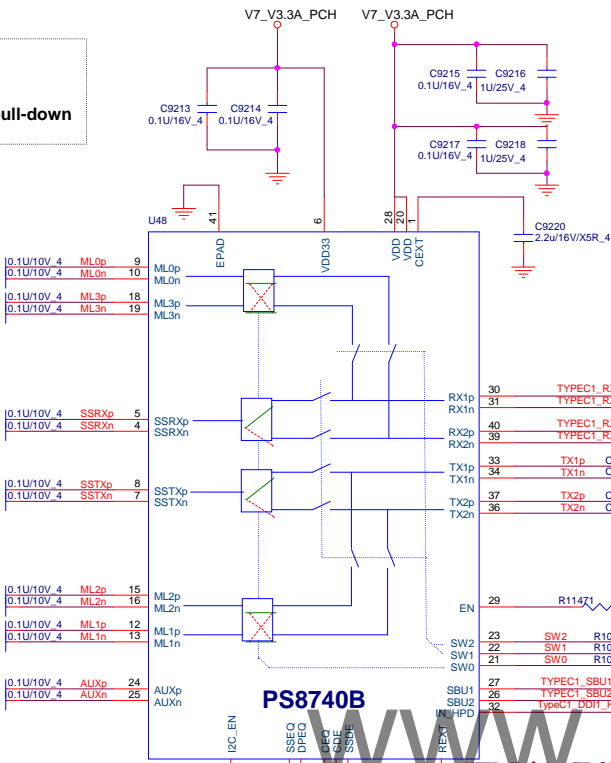
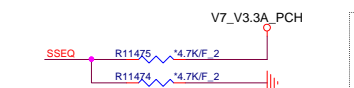
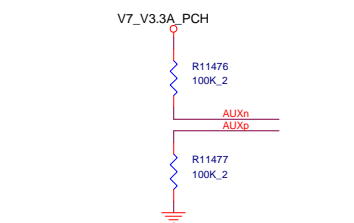
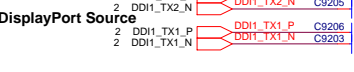
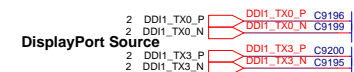




Apply and Check P/N & footprint

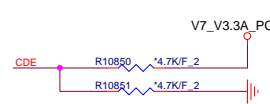
NEED Update FT 12/5

4/2 add charger LED function



```
USB HOST facing TX channel De-emphasis setting; Internal tied to
VDD33/2, 3.3V I/O.
SSDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)
```

```
USB HOST facing RX channel receiver equalization setting; Internal tied
to VDD33/2, 3.3V I/O.
SSEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)
```



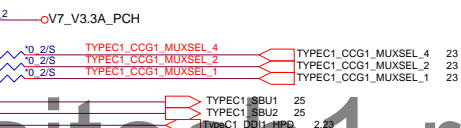
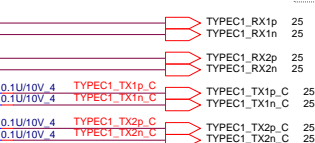
```
USB Type-C connector facing TX channel De-emphasis setting; Internal
tied to VDD33/2, 3.3V I/O.
CDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)
```



```
USB Type-C connector facing RX channel receiver equalization setting;
Internal tied to VDD33/2, 3.3V I/O.
CEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)
```



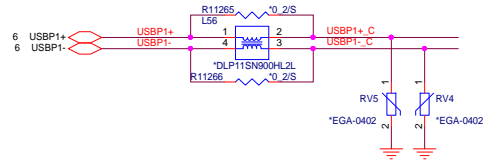
```
DP Receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)
```



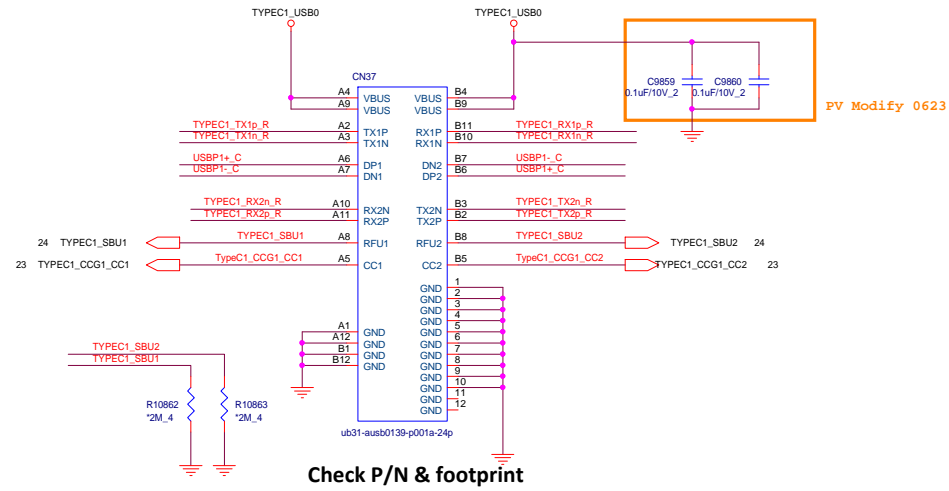
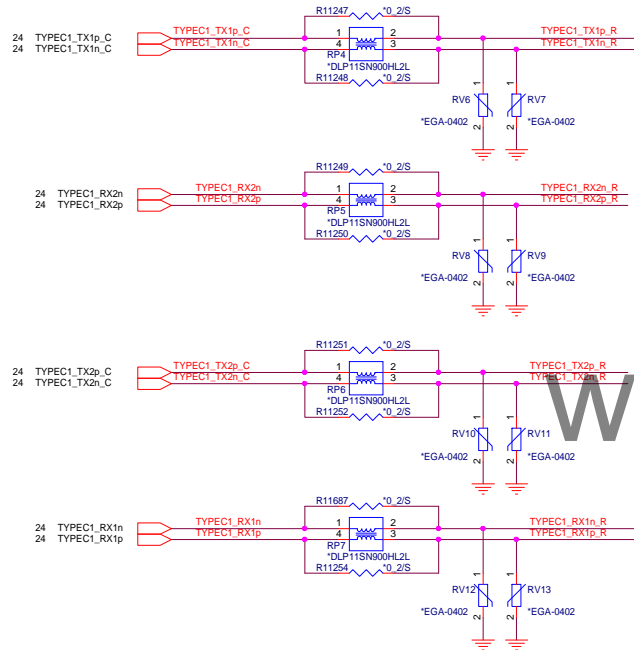
FS8740 Mode Selection				
SW2	SW1	SW0		
L	L	L	Chip Power Down	
L	L	H	Chip Power Down	
L	H	L	USB only on SS1 channels	
L	H	H	USB only on SS2 channels	
H	L	L	DP only; MLO on SRRX2	
H	L	H	DP only; MLO on SRRX1	
H	H	L	USB+2lanes DP;DP MLO on SRRX2	
H	H	H	USB+2lanes DP;DP MLO on SRRX1	

PS8740B Pin Control Mode

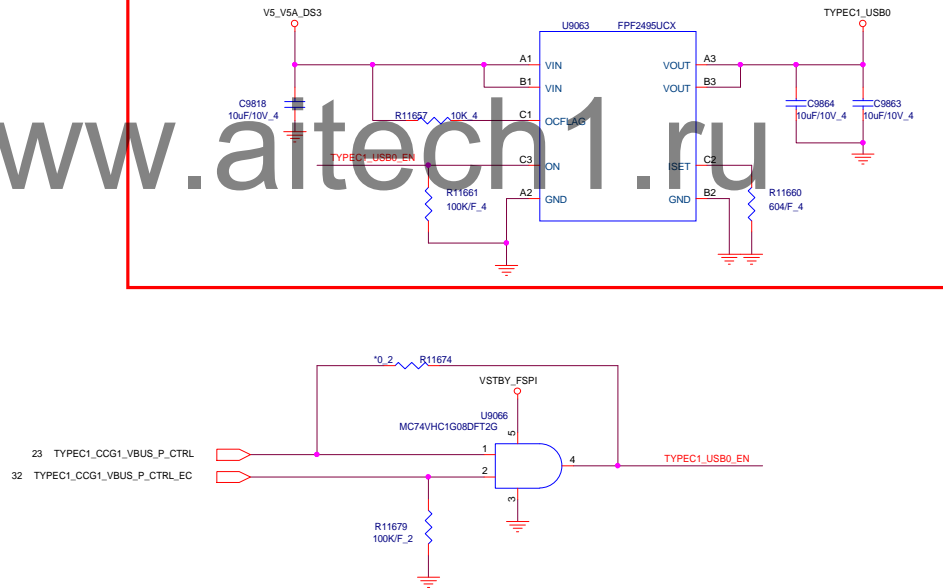
USB2.0 ESD



Type C1_HSIO_ESD



SI-2 Modify



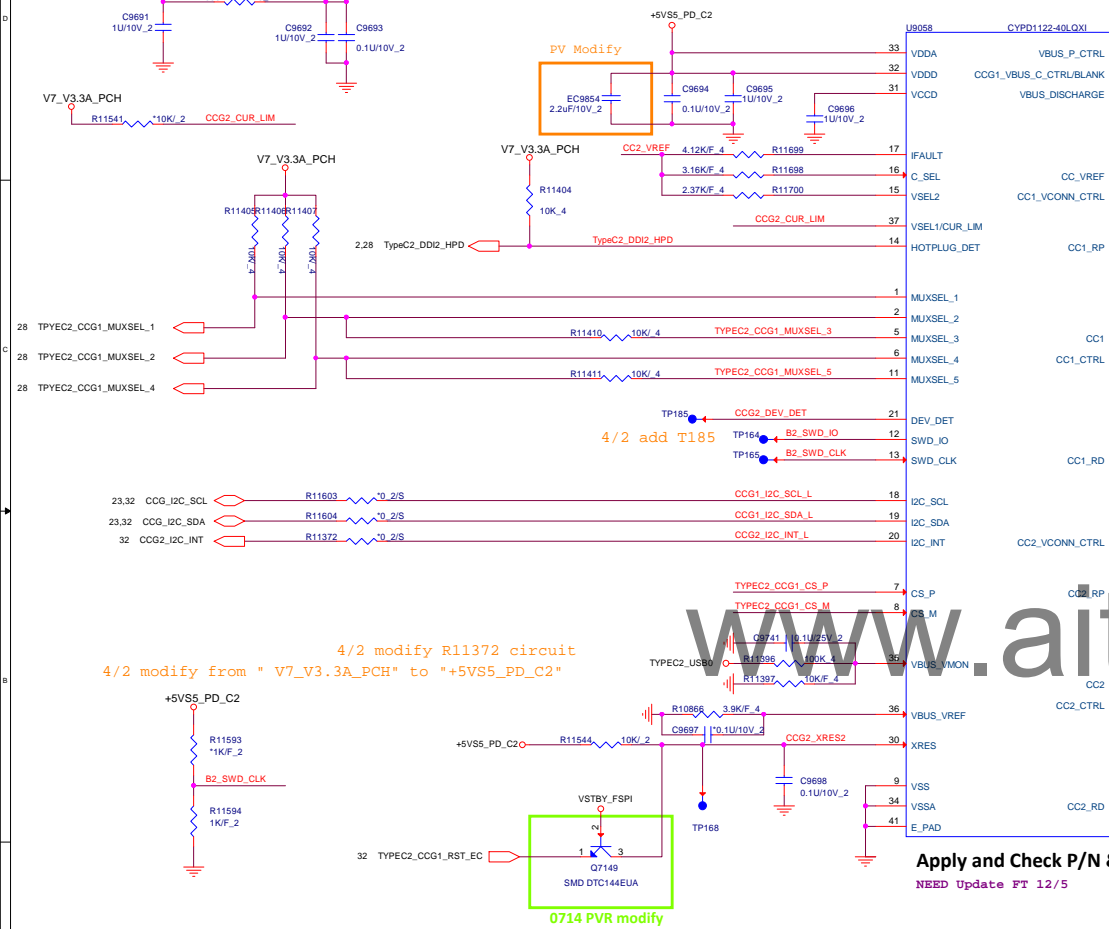
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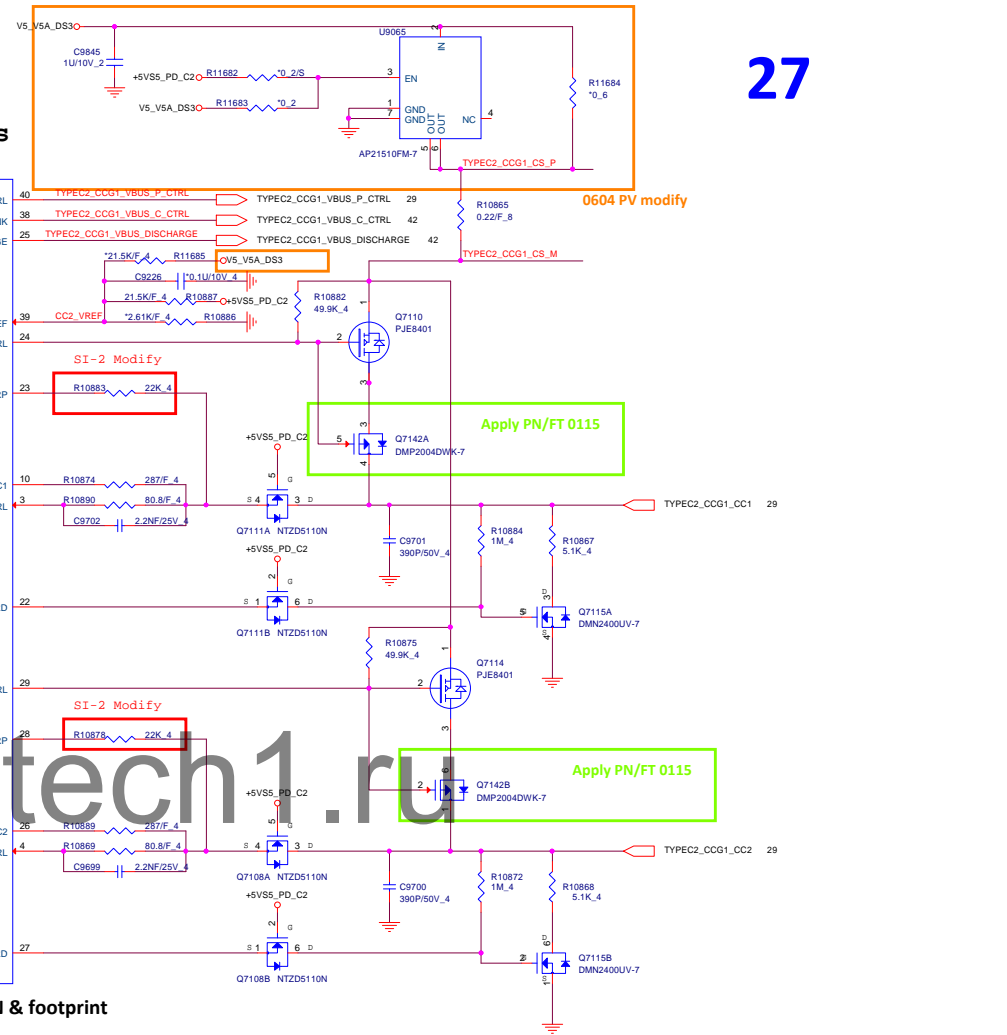
Size	Document Number	Rev
	VBUS Provider _1	A
Date:	Friday, August 28, 2015	Sheet 26 of 48

CCG1 Connections



Apply and Check P/N & footprint

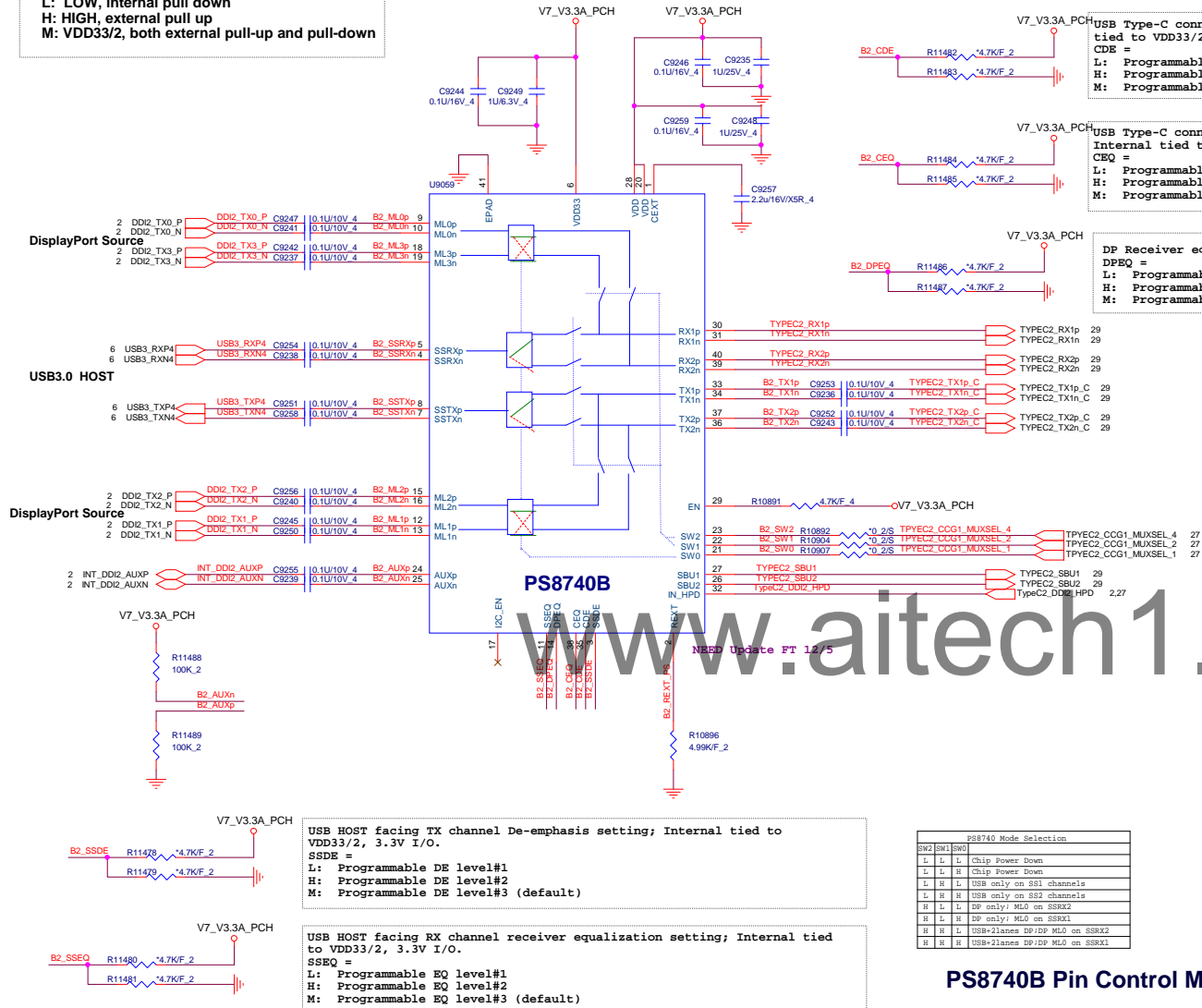
NEED Update FT 12/5



4/2 add charger LED function

3 Level Input:

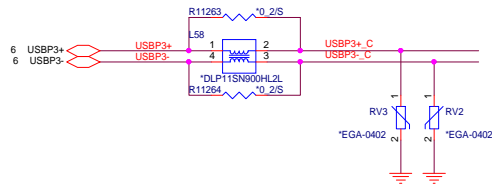
L: LOW, internal pull down
H: HIGH, external pull up
M: VDD33/2, both external pull-up and pull-down



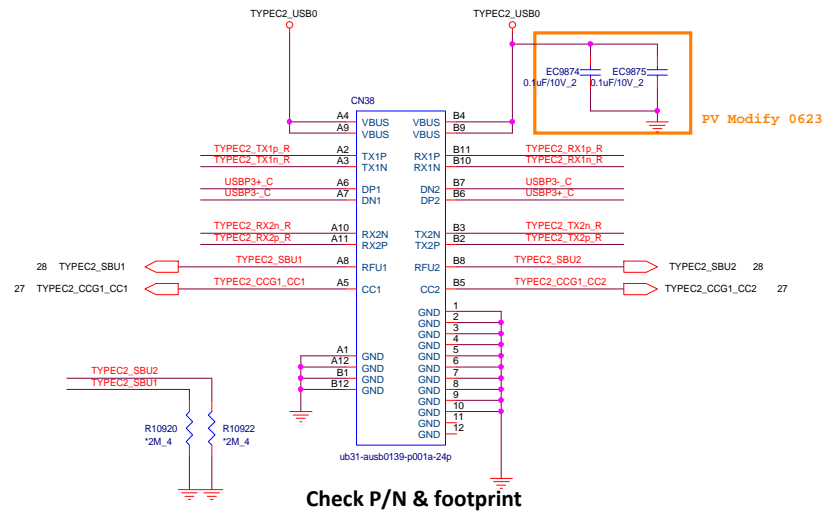
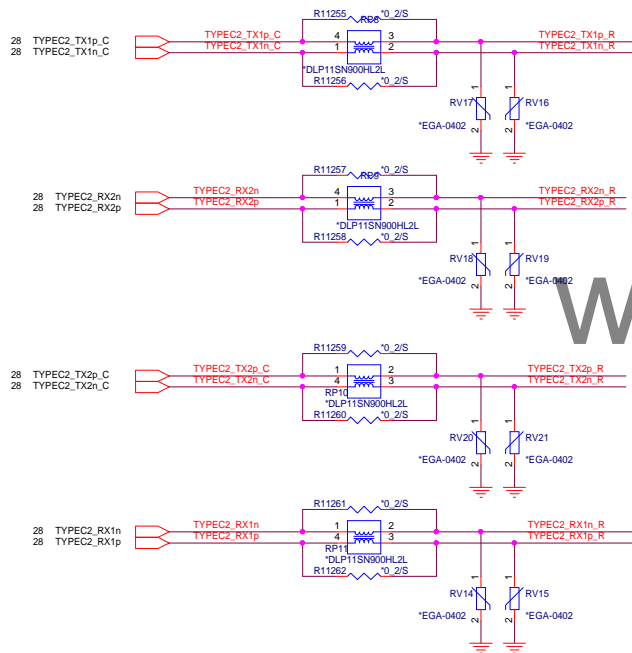
PROJECT : Millhone
Quanta Computer Inc.

Size Document Number
PS8740B Pin Control_2 Rev
A
Date: Sunday, August 30, 2015 Sheet 28 of 48

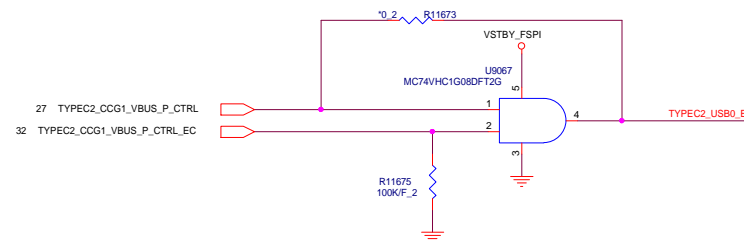
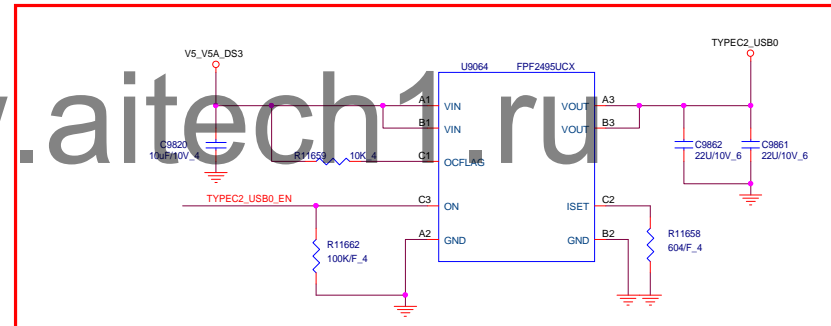
USB2.0_ESD




Type C2_HSIO_ESD



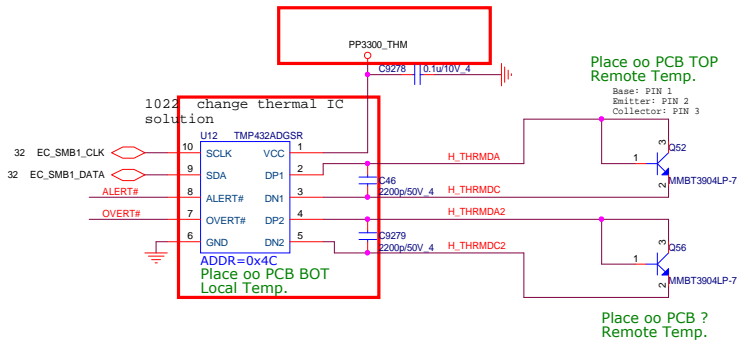
SI-2 Modify



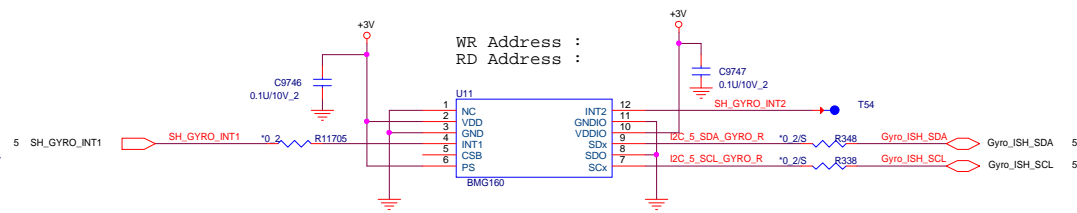
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 NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
	Size	Document Number	Rev
		VBUS Provider_2	A
Date: Friday, August 28, 2015		Sheet	30 of 48

Thermal Sensor(THM)

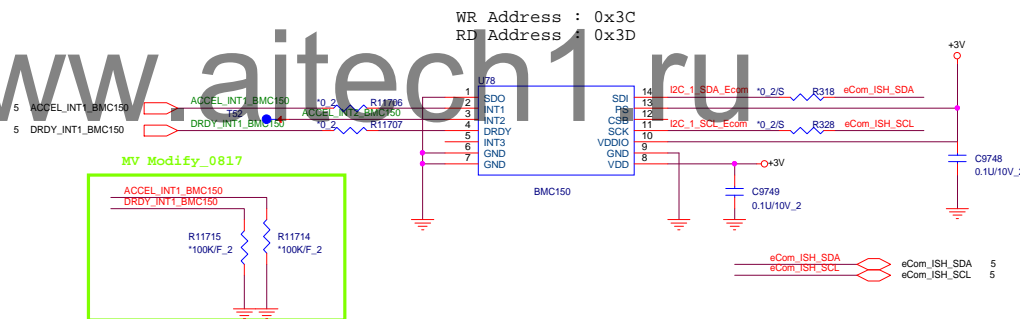


Gyroscope (BMG160)

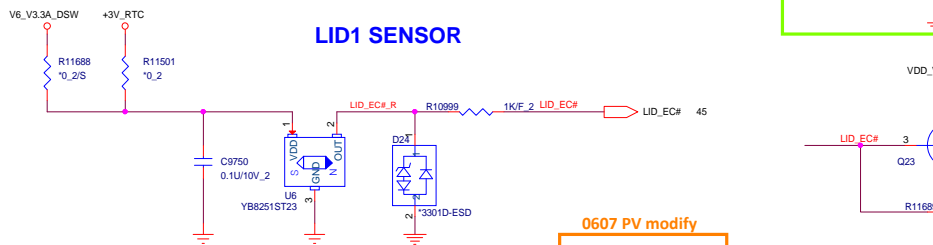


E-compass/Magnetometer/Accelerometer (BMC150)

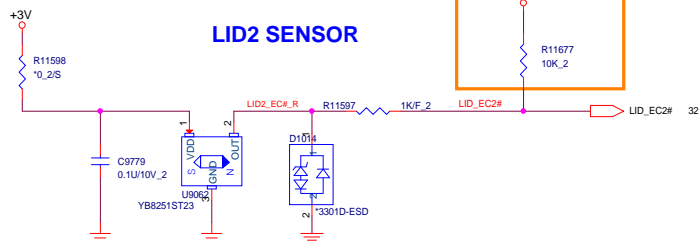
Keepout area is around 10mm



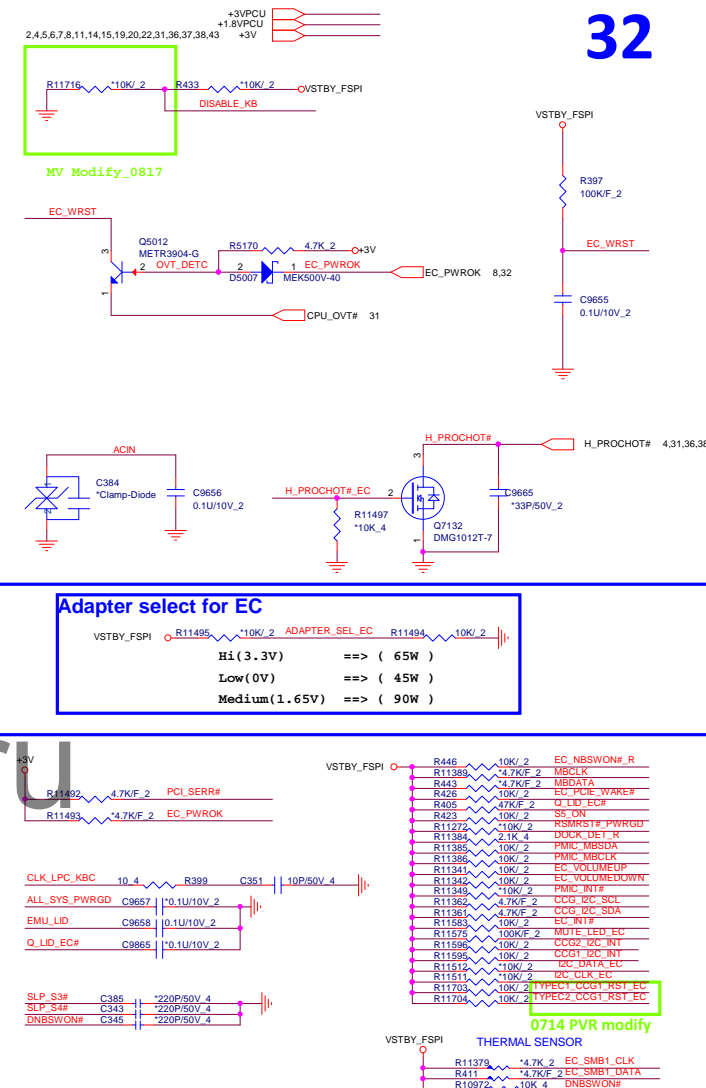
LID1 SENSOR



LID2 SENSOR



4/9 change net from "LID2_EC#_R" to "LID_EC#_R"



The schematic diagram shows the NBS HW board layout. Key components and connections include:

- EC_CT_UP** connected to **R10970** (4.7K F) and **V4_VCCIO**.
- Q7127** (MBIST3804T-7-F) connected to **EC_THRMTRIP#** (pin 4).
- EC_WRST** connected to pin 3.
- C9280** (Z20P150V_4) connected to ground.

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC ITE 8987	A

[illegible]

LDO3V  LDO3V 4,32,34,36,44,48

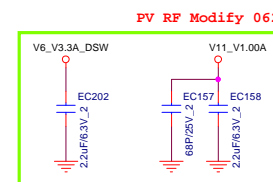
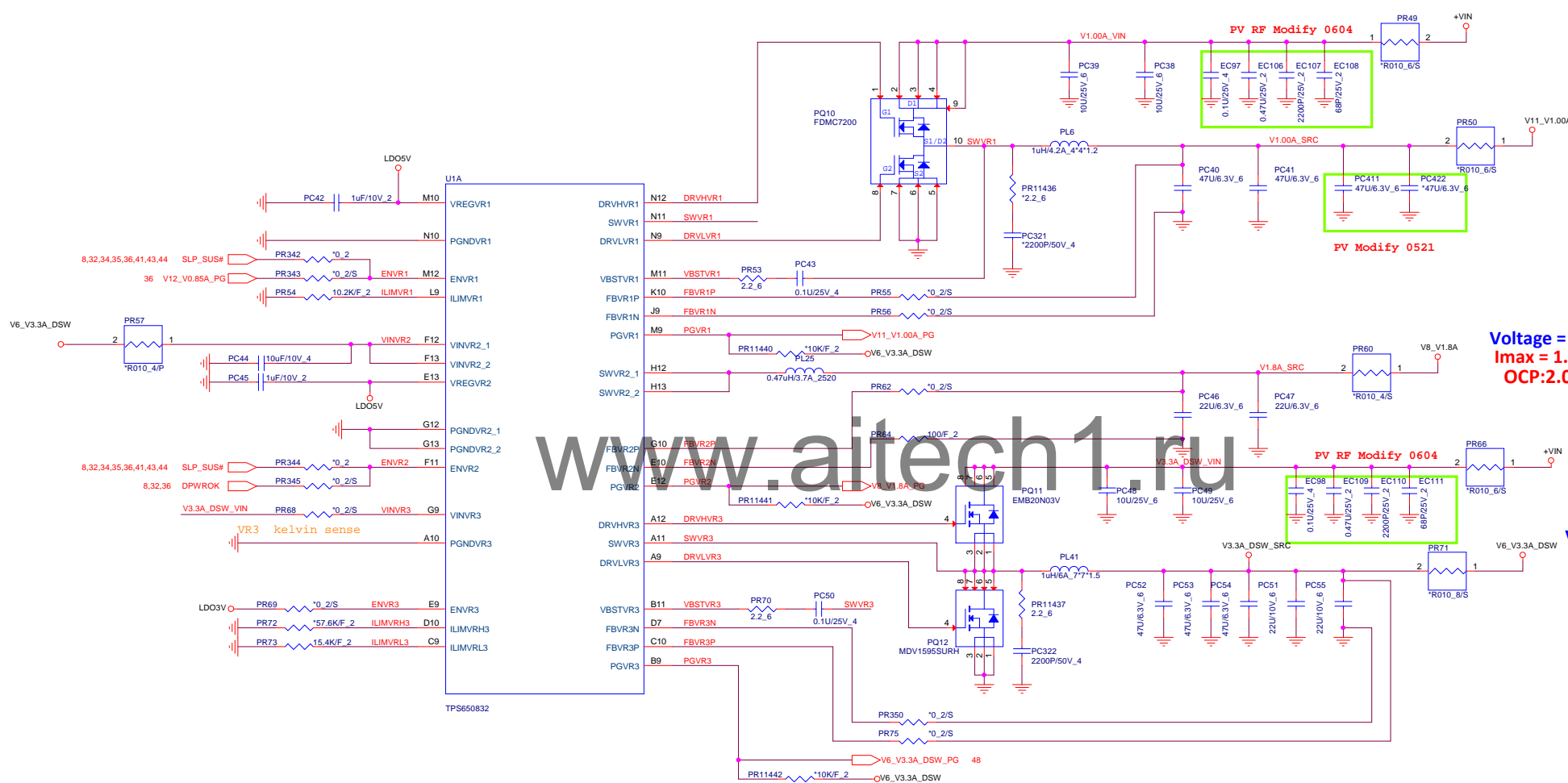
Max current : 2.6A

PV Modify 0618



PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number Charger (BQ24780)_45W	Rev A
Date:	Friday, August 28, 2015	Sheet 33 of 48



```

graph TD
    V6_V3.3A_DS_W[V6_V3.3A_DS_W] --- C1[4,8,10,18,23,27,31,32,35,36,40,41,43,46]
    V6_V3.3A_DS_W --- V3.3A_DS_W_SRC[V3.3A_DS_W_SRC]
    V3.3A_DS_W_SRC --- V11_V1.00A[V11_V1.00A]
    V3.3A_DS_W_SRC --- V1.00A_SRC[V1.00A_SRC]
    V11_V1.00A --- C2[5,10,11,36,44]
    V11_V1.00A --- V8_V1.8A[V8_V1.8A]
    V8_V1.8A --- C3[5,10,19,32,37,43,44]
    V8_V1.8A --- V1.8A_SRC[V1.8A_SRC]
  
```

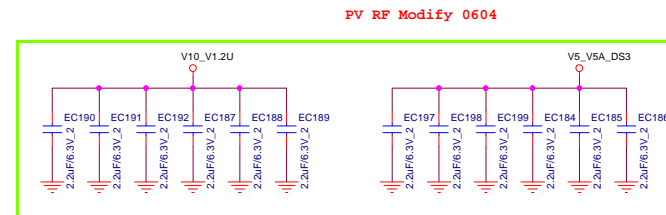
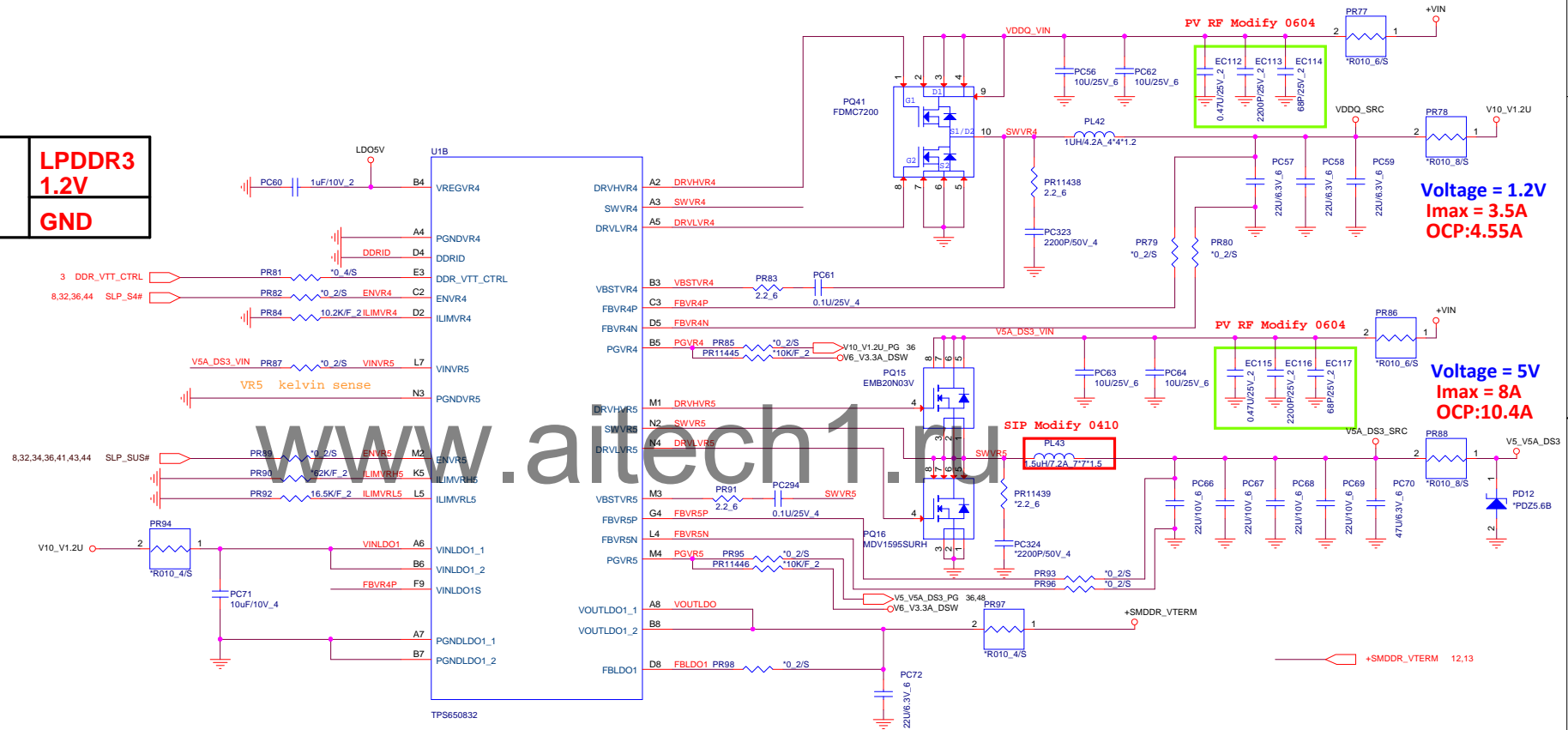
V6_V3.3A_DS_W 4,8,10,18,23,27,31,32,35,36,40,41,43,46
 V3.3A_DS_W_SRC
 V11_V1.00A 10,11,36,44
 V1.00A_SRC
 V8_V1.8A 5,10,19,32,37,43,44
 V1.8A_SRC



PROJECT : Millhone
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Size	Document Number System PMIC (TPS650832_1)	Rev A
Date:	Friday, August 28, 2015	Sheet 34 of 48

DDRID	LPDDR3
	1.2V
	GND

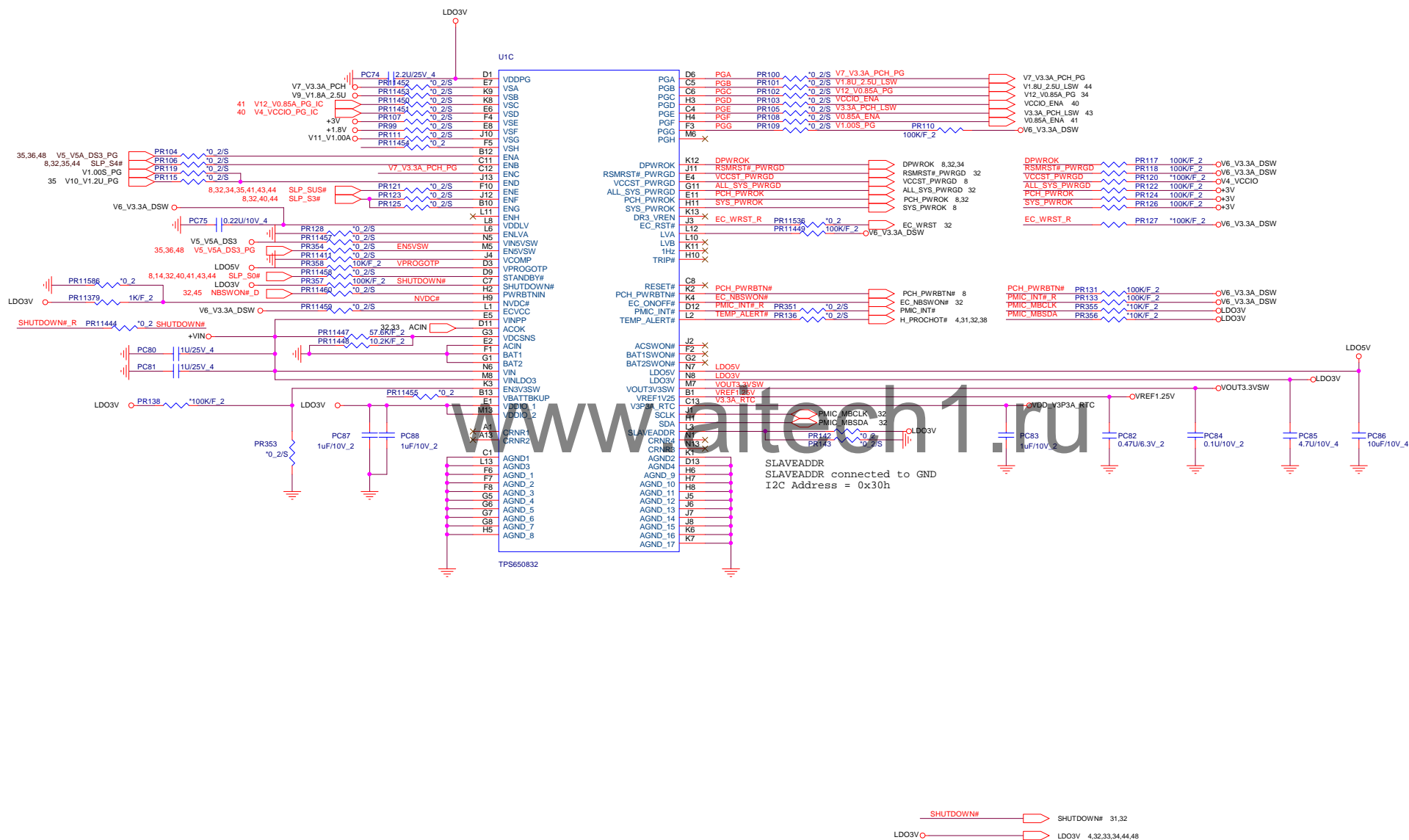


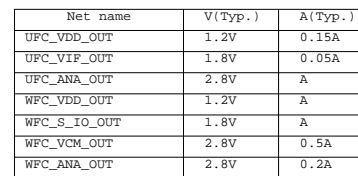
V5_V5A_DS3	23,25,27,29,36,38,39,42,43,44,48
V5A_DS3_SRC	
V10_V1.2U	10,12,13,44
VDDQ_SRC	
+SMDDR_VTERM	12,13
VOUTLDO	



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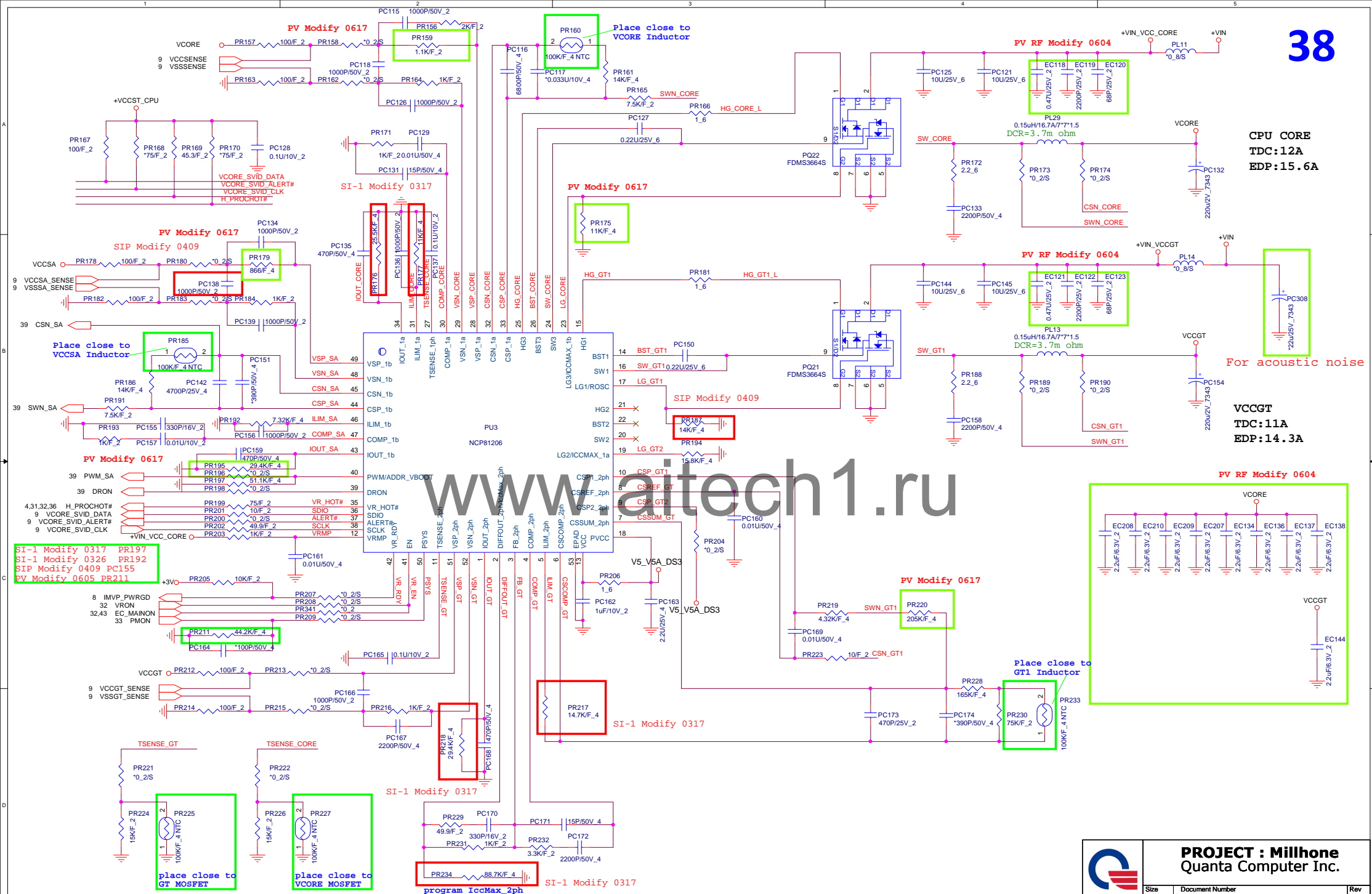
Size	Document Number	Rev
NB5 HW	System PMIC (TPS650832_2)	A
Date:	Friday, August 28, 2015	Sheet 35 of 48

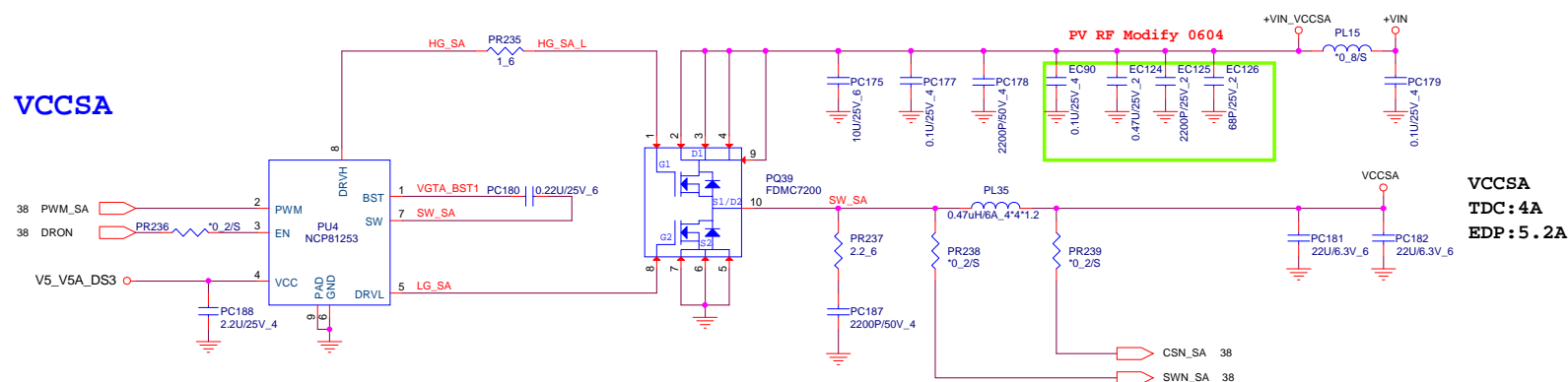




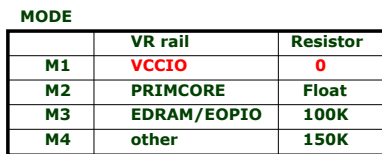
Net name	V(Typ.)	A(Typ.)
UFC_VDD_OUT	1.2V	0.15A
UFC_VIF_OUT	1.8V	0.05A
UFC_ANA_OUT	2.8V	A
WFC_VDD_OUT	1.2V	A
WFC_S_IO_OUT	1.8V	A
WFC_VCM_OUT	2.8V	0.5A
WFC_ANA_OUT	2.8V	0.2A

- | | |
|-----------------|---------|
| UFC_VDD_OUT | 37 |
| UFC_VDD_OUT_C7 | |
| WFC_VDD_OUT | 15,37 |
| WFC_VDD_OUT_G7 | |
| WFC_VCM_OUT | 15,37 |
| WFC_VCM_OUT_H4 | |
| WFC_ANA_OUT | 15,37 |
| WFC_ANA_OUT_B7 | |
| WFC_S_IO_OUT | 15,37 |
| WFC_S_IO_OUT_D7 | |
| UFC_VIF_OUT | 5,15,37 |
| UFC_VIF_OUT_A6 | |
| WFC_ANA_OUT | 15 |
| N1936A001 | |





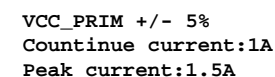
www.aitech1.ru



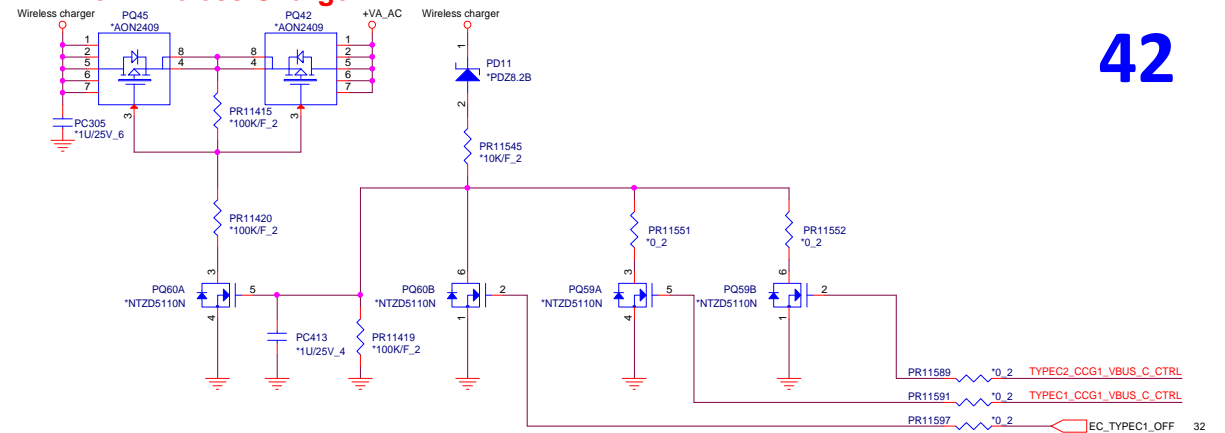
V4_VCCIO 2,7,10,32,36
+VCC_VCCIO_SRC



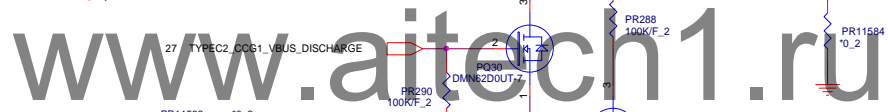
Size	Document Number +VCC_VCCIO (NB681)	Rev A
Date:	Friday, August 28, 2015	Sheet 40 of 48

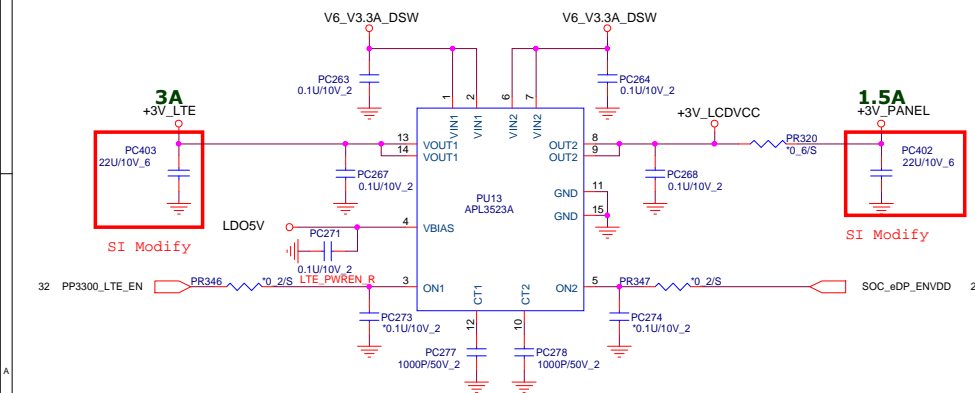
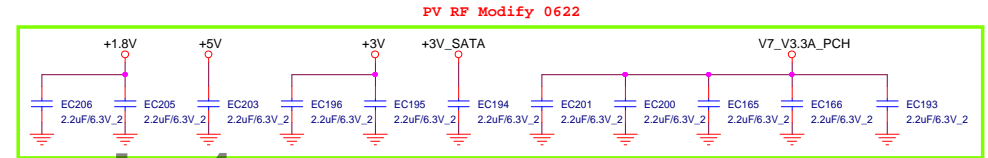
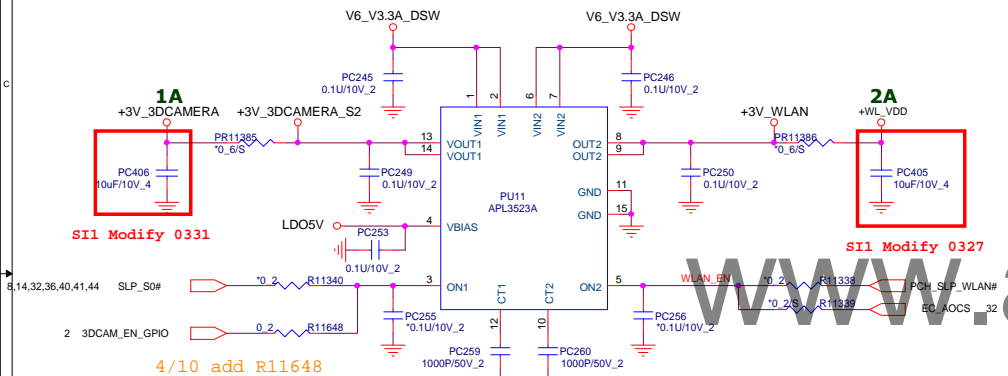
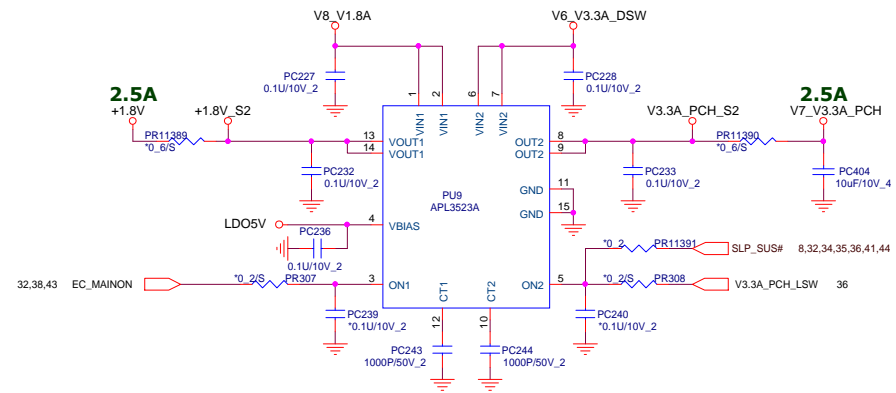
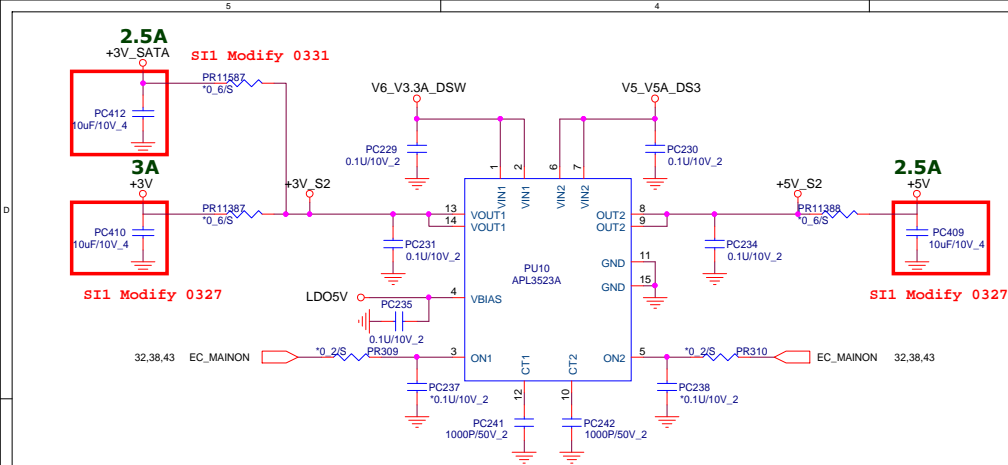


MODE		
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K



For TypeC PORT2





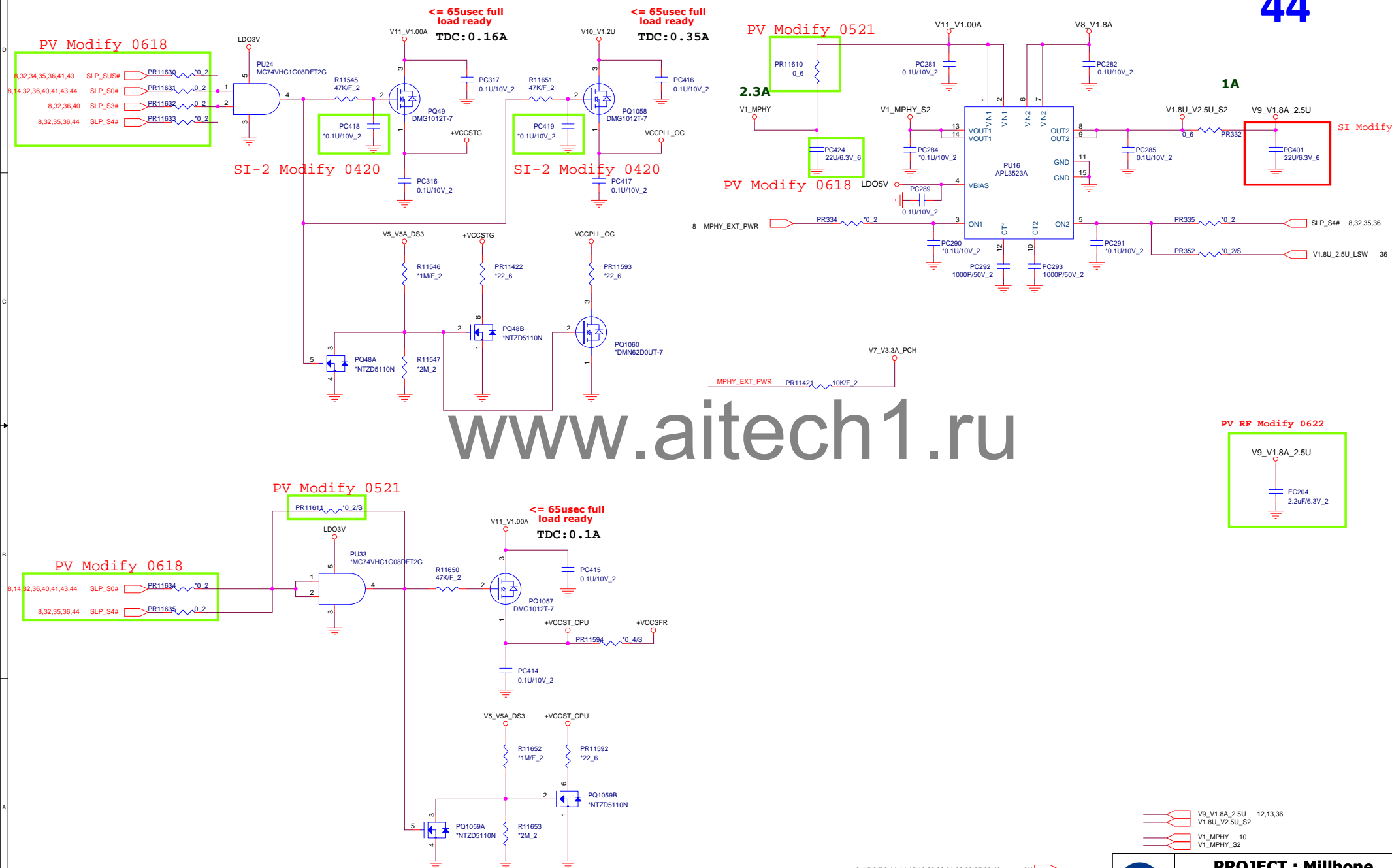
- +3V_3DCAMERA 16,37
- +3V_3DCAMERA_S2 17
- +3V_SATA 43
- +3V_S2 43
- +WL_VDD 18
- +3V_WLAN 18
- +3V_PANEL 14
- +3V_LCDVCC 14
- V7_V3.3A_PCH 2,4,5,6,8,10,14,18,19,23,24,27,28,36,37,44
- V3.3A_PCH_S2 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43
- +3V_S2 43
- +5V 20,43,45
- +5V_S2 43
- +1.8V 15,20,36
- +1.8V_S2 43

- 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43 +3V
- 20,43,45 +3V
- 14,33,34,35,36,38,39,40,41,48 +VIN
- +3VS5
- +5VS5
- +3VLAVCC



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Size	Document Number	Rev
	Load switch IC (APL3523A)	A
Date:	Friday, August 28, 2015	Sheet 43 of 48



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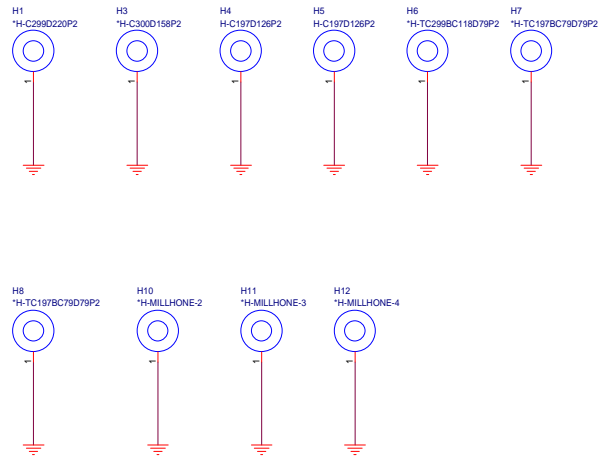
2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43
20,43,45
14,33,34,35,36,38,39,40,41,48
+3V
+3V
+3VS5
+5VS5
+3VLAVCC



PROJECT : Millhone
Quanta Computer Inc.

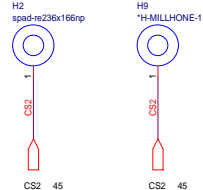
Size	Document Number	Rev
	Load switch IC (APL3523A)	A
Date:	Friday, August 28, 2015	Sheet 44 of 48

SCREW HOLE

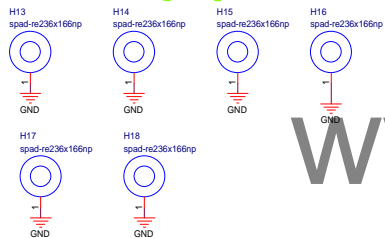


P-Sensor Spring

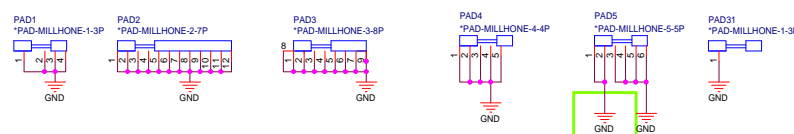
4/14 modify H2
footprint to spad-re236x166np



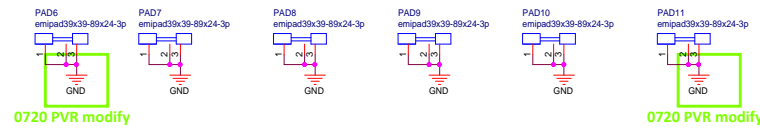
7/16 add gnd pad for RF



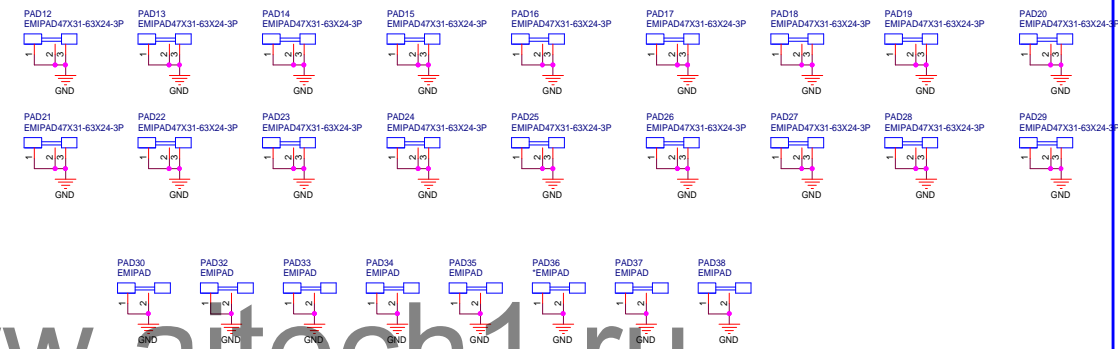
BOT SHIELDING PAD



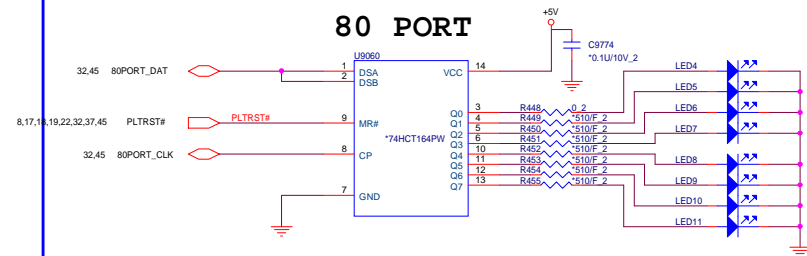
CLIP WLAN SHIELDING



CLIP THERMAL SHIELDING



80 PORT



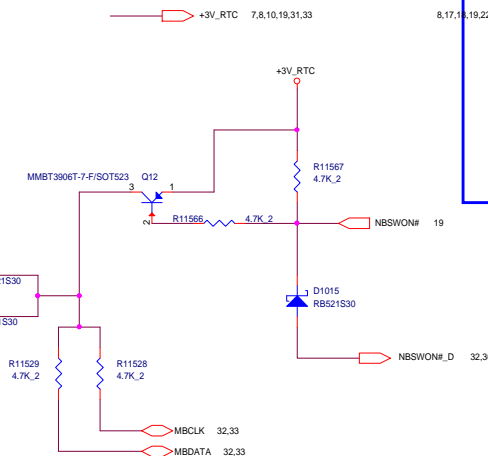
MV Modify_0817

Input	RD	CP	D	Output	Q
S0	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input	RD	CP	D	Output	Q _{n+1}	Q _{n+1}
S0	H	T	L	L	H	L
H	H	T	H	H	L	L

[1] H = HIGH voltage level;
L = LOW voltage level;
T = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.



Millhone Power up sequence

